QPLL – a Quartz Crystal Based PLL for Jitter Filtering Applications in LHC

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Abstract

A Quartz crystal based Phase-Locked Loop (QPLL) IC was developed for jitter filtering applications in the LHC experiments. The ASIC addresses the need of providing low-jitter clock reference signals to high-speed serializers, deserializers, high-resolution time-to-digital converters and analogue-to-digital converters. The device is to be used as a complement of the TTC system in all the situations where the TTCrx clock jitter proves to be excessive.

The QPLL was produced in prototype quantities and successfully tested. The ASIC was fabricated in a commercial 0.25 µm CMOS technology using radiation tolerant layout practices as well as Single Event Upset robust circuits.

The circuit and experimental results are discussed in detail in this work.

I. INTRODUCTION

The LHC experiments will use Gbit/s communication links for data transmission between the detectors and the data acquisition systems situated in the counting rooms. To simplify the synchronization of the detectors electronics these data links will, in the majority of the cases, run synchronously with the LHC master clock. The TTC system [1], [2] is used by all the LHC experiments to broadcast timing information. However, the phase-noise characteristics of the clock signals provided by the TTC system are not compatible with the jitter requirements of Gbit/s data serializers. To overcome this difficulty a Phase-Locked Loop based on a voltage controlled Quartz crystal oscillator (QPLL) was developed. The device locks to the LHC master clock signal (40.078686 MHz ±12 ppm) distributed by the TTC system and produces clock signals with low phase-noise capable of being used as frequency references for high-speed serializers. The QPLL can also be used as a timing reference for high resolution Time-to-Digital and Analogue-to-Digital Converters that require synchronization with the LHC clock reference.

To allow its use inside the LHC detectors, the ASIC was fabricated in a commercial 0.25 µm CMOS technology using radiation tolerant layout practices as well as Single Event Upset (SEU) robust circuits.

In this work, after a brief overview of the QPLL functionality, the operation principles of the circuit will be described. The paper also reports on data transmission tests done with Gbit/s serializers clocked by the QPLL.

II. CIRCUIT OVERVIEW

The block diagram of the QPLL IC is shown in Figure 1. The circuit is essentially a Phase-Locked Loop implemented around a Voltage-Controlled Crystal Oscillator (VCXO). Such a PLL has intrinsic low phase-noise and narrow loop-bandwidth being ideal for jitter filtering applications. An advantage of this configuration is that even in the absence of the reference signal the device will always produce clock outputs with frequencies very close to the locked frequency. However, due to the narrow frequency range imposed by the quartz resonator a custom crystal is required.

The circuit takes the LHC clock as an input and generates, by frequency multiplication, three synchronous clock signals. Two frequency multiplication modes are available: In one mode, the input clock frequency is multiplied by 1, 2 and 4 while in the other mode, the multiplication factors are 1, 1.5 and 3. Each frequency multiplication mode requires a custom tailored crystal.

All the QPLL clock outputs are LVDS while the reference clock input can be either CMOS or LVDS. To facilitate the interface with the TTCrx and other circuits, all the CMOS inputs are 5V tolerant.

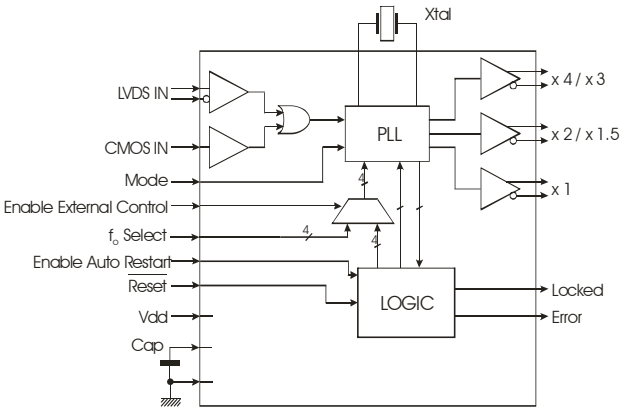

Figure 1: QPLL block diagram

It is possible to disable the PLL operation and use the QPLL as a simple clock source. In this mode, the oscillation frequency can be adjusted with four bits resolution within the VCXO digital tuning range (approximately 78 ppm).

III. CIRCUIT OPERATION

The heart of the ASIC is the PLL whose block diagram is represented in Figure 2. The PLL is of the bang-bang type [3]. In this type of PLL circuits, the phase detector gives only

discrete information about the sign of the phase error existing between the internally generated clock and the reference signal. That is, at every clock cycle the VCXO signal is reported either early or late. Due to the low value of the loop bandwidth required and to the extremely low gain of the VCXO circuit, a phase locked-loop employing the more classical three-state phase detector [4], [5] would result in loop filter component values that would be difficult to integrate and in control voltages, that taken blindly, would lead to saturated behaviour of the PLL. Additionally, the VCXO circuit is well suited for a two-branch control loop (as shown in Figure 2), which allows almost independent optimisation of the proportional and integral parts of the loop. For this reason, the bang-bang type was preferred.

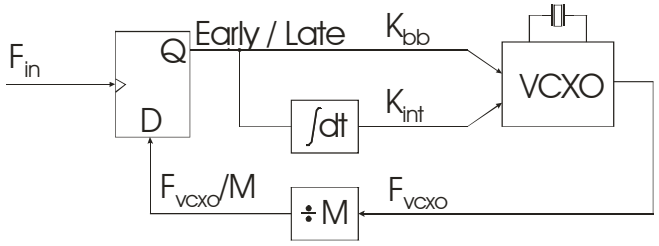

Figure 2: QPLL architecture

In the loop, the integral branch (K_{int}) guarantees that the PLL tracks the mean value of the input signal frequency while the proportional part (K_{bb}) makes sure that the instantaneous VCXO frequency and phase are always "bracketing" that of the incoming signal. In principle, minimizing the proportionality constant K_{bb} will reduce the tracking jitter. In practice K_{bb} cannot be chosen completely independent of K_{int} and a minimum value of the ratio K_{bb} / K_{int} has to be guarantied to maintain the system stable [3].

A. Controlling the VCXO frequency

The simplified schematic diagram of the VCXO is represented in Figure 3 A). It consists of a Pierce oscillator with two "variable" capacitors for frequency tuning. These capacitors allow the crystal oscillator to be used as a voltage controlled oscillator in the QPLL.

In the very big majority of the cases, a crystal is used to set a reference frequency. Ideally, for such applications, the crystal should be loaded by an infinite capacitance ("short circuit"). In this case, the circuit oscillation frequency would be given exactly by the resonance frequency of the crystal. However, practical oscillator circuits have finite loading capacitances and the combination of the pair crystal and oscillator circuit will oscillate at a frequency that is higher than the crystal resonance frequency. This is expressed in mathematical terms by the following equation:

$$f_O = f_m \sqrt{1 + \frac{C_m}{C_{circuit}}}$$

were, f_O is the circuit oscillation frequency, f_m is the crystal resonance frequency (infinite load capacitance), C_m is the crystal motional capacitance and $C_{circuit}$ is the capacitance associated with the oscillator, the IC and the crystal packages and the PCB routing.

This equation shows very clearly that it is possible to control the oscillator frequency by varying the circuit capacitance. One might be tempted to think that a large variation of frequency can be achieved. However, in practical circuits C_m is orders of magnitudes smaller than $C_{circuit}$ restricting dramatically the tuning range to at best some hundreds of Parts Per Million (ppm) since the intrinsic circuit components and parasitics limit the minimum achievable value of $C_{circuit}$. For example in the case of the QPLL circuit C_m is equal to 5.9 fF and $C_{circuit}$ equal to 4.5 pF at the centre of its range with maximum and minimum values of 5.5 pF and 3.4 pF, respectively.

The reduced influence of the circuit capacitance is an advantage since the oscillation frequency becomes essentially determined by the crystal. For VCXOs this is translated in a low VCO gain facilitating the design of low bandwidth PLLs required in jitter filtering applications. The small frequency range of VCXOs maps directly into a small PLL locking range requiring custom crystal tuning[1] during manufacturing to guarantee phase and frequency lock.

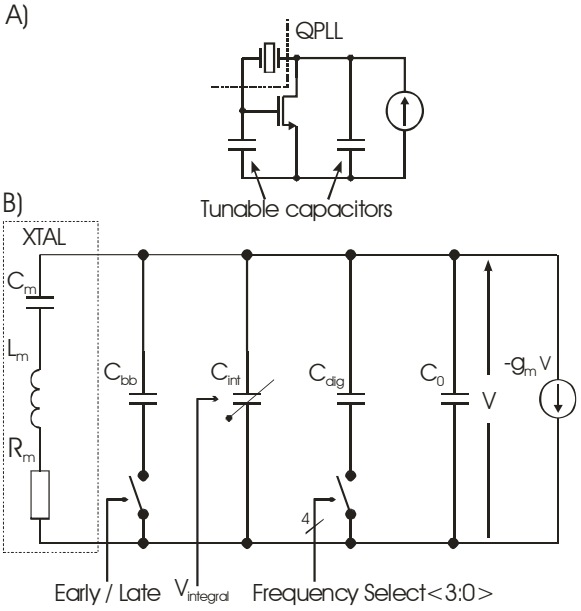

Figure 3: A) VCXO simplified circuit, B) VCXO model.

1) Capacitance tuning mechanisms

The electric model of the crystal and oscillator is represented in Figure 3 B). The quartz crystal is modelled by the motional capacitance C_m, the motional inductance L_m, and the motional resistance R_m. When an oscillation is present on the resonator, part of the energy is dissipated on R_m during each cycle. If this energy is not restored by the active part of the circuit, the oscillations will eventually stop. When the circuit is operating in its steady state, the amount of energy

[1] Crystal frequency tuning to a given nominal load capacitance is a standard service offered by quartz crystal manufactures.

dissipated per cycle is exactly restored by the active circuit. In the circuit of Figure 3 B) this is modelled by the presence of the $-g_m V$ current generator.

The QPLL includes three mechanisms to control the circuit capacitance. In the model, they are represented by the capacitors, C_{bb}, C_{dig} and C_{int} and their associated switches and control voltage. An additional capacitor C_O is used to represent the capacitances associated with the active circuit and any stray capacitances due to packaging and PCB routing. Capacitor C_{bb} is used to implement the proportional term of the PLL control loop. Its associated switch is under direct control of the phase detector. The switch closes every time the VCXO phase is detected early reducing the oscillation frequency and, conversely, the switch opens if the VCXO phase is detected late. This mechanism allows phase and frequency tracking. Switching on and off this switch corresponds to a frequency jump of approximately 456 Hz. Theoretically this should result in a tracking jitter of no more than 3 ps (due to the proportional branch alone).

Capacitor C_{int} is part or the integral branch of the control loop and its value is controlled by the voltage produced by the loop-filter. This is a continuously tuneable capacitor implemented by a capacitor working in the accumulation region [6]. Its value ranges from 3 pF to 3.8 pF for a control voltage between 0 V and 1.6 V.

A third method of frequency control is implemented by a group of four binary weighted capacitors and their associated switches. They are represented in the equivalent circuit by C_{dig}. These capacitors are not under the direct control of the PLL control loop and their function is to centre the VCXO free running oscillation frequency.

2) Frequency centring .

In the QPLL, lock acquisition is done in two phases. The first phase consists of a frequency centring operation while the second phase is a standard PLL frequency pull-in and phase lock cycle.

After start-up, reset or in the case the PLL detects it is operating unlocked a frequency centring cycle is initiated. During such a cycle, the PLL control is disabled. That is, the proportional part of the PLL control loop is disabled and the integral capacitor control voltage forced to its mid range value. A binary search is then done switching on and off the binary weighted capacitors C_{dig} and a simple frequency-only comparator gives a frequency high/low indication. Once the capacitor settings that result in the closest operation frequency to that of the incoming signal are determined, control is passed to the PLL for final frequency and phase-lock acquisition.

The digital tuning range is around 3.2 kHz (78 ppm) while the analogue range is 2.6 kHz (66 ppm) resulting in a total locking range of 5.8 kHz (145 ppm). One should interpret the digital tuning range as a frequency "trim" so that the LHC frequency should fall inside that band for nominal operation conditions. Along the same lines, the analogue tuning range represents the margin that the QPLL has to track the LHC signal, power supply and temperature variations.

IV. DEALING WITH RADIATION EFFECTS

The QPLL uses well established techniques to deal with total dose radiation effects [7], [8]. As it is well known these techniques use a combination of factors to produce total dose robust circuits: first the intrinsically small gate oxide thickness of the technology guarantees that the threshold shifts of the transistors are minimal and second, the use of enclosed devices and guard rings prevents leakages within and in between devices. However, these techniques do not fully protect the circuit against Single Event Upsets (SEU).

In the QPLL, SEUs are dealt with a diversity of techniques. In the majority of the cases triple modular redundancy (majority voting) circuits are used. For example the state machine that decides if a frequency centring cycle must or not be done uses this type of circuits. However, some of the decisions must be taken based on the state of a single signal and simple voting is not enough to resolve the situation. For example if the signal that indicates that the PLL is running locked was momentarily disturbed by an SEU this could be enough to initialise a frequency centring cycle resulting in a relative long dead time. To guarantee that this doesn't happen, decisions that are critical to the circuit operation always pass through a confirmation state before they are executed. This gives time for the circuit to recover from the disturbing event and not to react in case the reported status was caused by an SEU on that signal. Additionally, some signals like the PLL lock indication are statistical in nature and need "filtering" before being fed as status signals to the control state-machines. For example, if the PLL is running locked, for it to be considered unlocked it is necessary for the PLL "locked" signal to be "0" for at least 64 consecutive clock cycles. This type of "filtering" is done by counters which can obviously be also subject to SEUs. The state-machine monitoring the status of these counters only produces an "unlocked" indication in case these counters report the same value. In case they disagree they are reset. Such an action is taken because it is the one that will have the smallest impact on the system operation. That is, it is better to wait 64 clock cycles to confirm that the PLL is in fact unlocked than to restart a frequency centring cycle which will take about a millisecond to complete.

To summarise, single event upsets are dealt with by either using majority voting circuits, by waiting for confirmation that a "critical" action needs in fact to be taken or finally in case of doubt by taking the action with the smallest impact on the system operation.

V. EXPERIMENTAL RESULTS

Several QPLLs were tested with five samples provided by the crystal vendor and tuned to four times the LHC frequency (the VCXO operation frequency). The crystal specification is given in Table 1. The tests were done with crystals cut for a loading capacitance of 3.75 pF which was the estimated circuit capacitance used to order these samples. The actual capacitance was determined by the tests with the samples and is given in Table 1. For the sample crystals, the VCXO free-running frequency is in average -41 ppm away from the

design target value (but less than 27 ppm among each other). The objective was to keep the frequency within ±25 ppm relatively to the LHC frequency. This discrepancy is mainly a consequence of the under estimation of the loading capacitance.

Table 1: Quartz crystal specification

Description	Typical	Min.	Max.	Unit
Crystal type	Inverted mesa AT-Cut			
Resonance mode	Fundamental			
Load Frequency	160.314744			MHz
Load Capacitance	4.48			pF
Frequency Tolerance at 25°C		-18	18	ppm
Motional Capacitance		4.2		fF
Static Capacitance	2.8			pF
Drive Level			100	µW
Operating Temperature Range		0	60	°C
Series Resistance at 25°C			35	Ohm
Drift over OTR		-10	10	ppm
Aging first year			± 3	ppm
Package type	SMD ceramic CC1F-T1A			

B. *Jitter*

The QPLL was connected to the clock output of the TTCrx to evaluate its jitter filtering performance. When operating with high density data and triggers the TTC system produces, at the output of the TTCrx, a clock signal with a cycle-to-cycle jitter of 76 ps RMS and 650 ps PP. The tests done so far show that those jitter levels can be reduced by the QPLL to 22 ps RMS and 206 ps PP, respectively (see Figure 4).

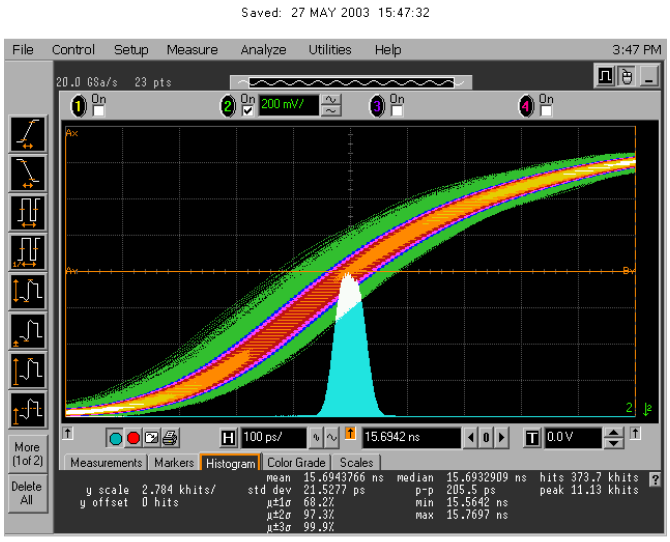

Figure 4 Long term jitter histogram for the QPLL driven by the TTCrx with high density data.

C. *Data transmission tests*

One of the main aims of the QPLL development is to allow the use of the TTCrx as a clock source for Gbit/s data links once its clock signal is jitter filtered by the QPLL. To prove this concept, a test was done whose test set-up is schematically represented in Figure 5.

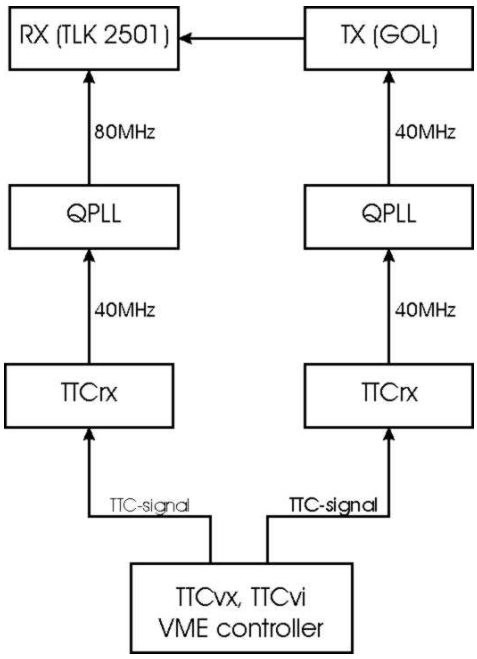

Figure 5 : BER test set-up

As shown in Figure 5, two QPLLs were used to independently serve as clock references for the GOL serializer [9], [10] and the TLK 2501 deserializer [11]. The GOL was clocked with the QPLL 40 MHz clock output while the deserializer was clocked by the 80 MHz output. On their turn, the two QPLLs received their reference clock signals from two TTCrxs that were driven by a TTC system composed of a TTCvx, a TTCvi and a VME controller [1], [2]. To maximize the amount of jitter on the TTCrx clock outputs during the test, both data and triggers were sent over two optical channels (TTC-signals in the figure) with a maximum trigger rate of approximately 400 kHz (limited by the test set-up). This increases the TTCrx clock jitter to the levels mentioned before. The test was run continuously during one week at 1.6 Gbit/s without any transmission error.

VI. SUMMARY

A jitter filtering Phase Locked-Loop based on a quartz crystal oscillator was developed by the CERN micro-electronics group and successfully tested. Jitter measurements and data transmission tests prove that the QPLL can be used to drive high speed data serializers using the TTCrx clock as a reference. The jitter levels present on the QPLL clock outputs are also compatible with high resolution Time-to-Digital converters and Analogue-to-Digital converters.

VII. REFERENCES

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