

# QPLL Manual

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## *Quartz Crystal Based Phase-Locked Loop for Jitter Filtering Application in LHC*

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**Preliminary**

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<b>Introduction</b>	<b>5</b>
Features:	5
<b>OPERATION</b>	<b>6</b>
QPLL operation modes	7
Mode 0:	7
Mode 1:	7
Mode 2:	8
QPLL Signals	10
Timing	12
<b>QPLL pinout</b>	<b>13</b>
Pin assignments	13
<b>Crystal specification</b>	<b>15</b>
<b>Power Reduction Network</b>	<b>16</b>
QPLL excess jitter	16
Recommended network:	16
<b>Power supply sensitivity</b>	<b>17</b>
Static phase error	17
VCXO free-running oscillation frequency	19
<b>PCB Layout recommendations</b>	<b>20</b>
Frequency pulling considerations	20
Layout	21
Procedure to verify the PCB parasitic capacitance	22

## Summary of Changes

### Version 1.3:

Figure 2 updated.

### Version 1.2:

Figure 2 updated.

### Version 1.1:

This version of the manual applies to both QPLL2 and QPLL3. Both versions of the ASIC are functionally identical. However QPLL3 has a higher tolerance to ionizing radiation (total dose). It is thus recommended to restrict the use of the QPLL2 to systems where radiation tolerance is not a concern.

#### Manual changes:

- Crystal specifications changed. See “Crystal specification”;
- Addition of the section “Power Reduction Network”;
- Section: “PCB Layout recommendations”: expanded.

### Version 1.0:

This version of the manual reflects the changes that were introduced in the second version of the QPLL. To avoid any confusion with the previous version, these chips are now marked as “**QPLL2**”.

QPLL version 2 is 100% pin compatible with version 1. Except for operation mode 2 (see QPLL operation modes) the two versions are functionally identical. Users that already developed boards based on version 1 will be able to simply replace each QPLL by a QPLL2.

#### ASIC changes:

- The frequency select bus was expanded to 6 bits;
- Pins **autoRestart** and **~reset** become dual function;

#### Manual changes:

- Section “OPERATION”: expanded;
- Section “Timing”: new;
- Section “Crystal specification”: new.
- “Power supply sensitivity”: new;
- Section: “PCB Layout recommendations”: expanded;
- Section “Procedure to verify the PCB parasitic capacitance” new.

### Version 0.3:

- Dielectric thickness corrected in Figure 10 (recommend layout).

### Version 0.2:

- Legend corrected in Figure 10 (recommend layout).

**Version 0.1:**

- Section “PCB Layout recommendations” added to the manual.

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## INTRODUCTION

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The QPLL is a Quartz crystal based Phase-Locked Loop. Its function is to act as a jitter-filter for clock signals operating synchronously with the LHC bunch-crossing clock. Two frequency multiplication modes are implemented: 120 MHz and 160 MHz modes<sup>1</sup>. In the 160 MHz mode, the ASIC generates three clock signals synchronous with the reference clock at 40 MHz, 80 MHz and 160 MHz while in the 120 MHz mode the synthesized frequencies are 40 MHz, 60 MHz and 120 MHz. In both cases, the highest frequency is generated directly from a Voltage Controlled Crystal Oscillator (VCXO) and the lower frequencies are obtained by synchronous division. The two frequency multiplication modes require Quartz crystals cut to the appropriate frequencies.

### Features:

- Phase-Locked Loop based on a Voltage Controlled Crystal Oscillator
- Designed to frequency and phase-lock to the LHC master clock:  $f = 40.0786$  MHz
- Locking range:  $\Delta \approx \pm 3.7$  KHz around  $f = 40.0786$  MHz
- Loop bandwidth:  $< 7$  KHz
- Locking time – including a frequency calibration cycle (mode 1):  $\sim 180$  ms
- Locking time – excluding a frequency calibration cycle (mode 0):  $\sim 250$   $\mu$ s
- Two frequency multiplication modes:
  - $\times 1$ ,  $\times 2$  and  $\times 4$
  - $\times 1$ ,  $\times 1.5$  and  $\times 3$
- Output jitter:  $< 50$  ps peak-to-peak for an input signal jitter less than 120 ps RMS
- Reference clock input levels:
  - LVDS
  - CMOS single-ended, 2.5 V to 5 V compatible
- Three LVDS clock outputs
- Package: LPCC-28 (5 mm  $\times$  5 mm, 0.5 mm pitch)
- Power supply voltage: 2.5V nominal (allowed operation range 2.4V to 2.7V)
- Phase error sensitivity to the power supply voltage: less than  $-0.72$  ps/mV
- VCXO free-running frequency sensitivity to the power supply: 0.14 Hz/mV (typical)
- Power consumption: 100 mW
- Radiation tolerant
- 0.25  $\mu$ m CMOS technology
- Crystal: A quartz crystal is provided with each QPLL.

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<sup>1</sup> Please note that frequency numbers in this document are often rounded to the nearest integer. This is just a simplification to facilitate document reading. In fact, these numbers should be interpreted to be the exact multiples of the LHC bunch-crossing clock frequency.

## OPERATION

The QPLL uses the LHC bunch-crossing clock as the reference frequency. This signal can be feed to the ASIC either in CMOS or LVDS levels (please refer to Figure 1). Selection of which input to use is simply done by forcing the unused clock input to logic level “0” (notice the use of the OR function in the reference clock signal path in the block diagram). The three clock outputs are LVDS signals and their frequency depends on the “mode” input. When “mode” is set to “0” the output clock frequencies are: 40 MHz, 60 MHz and 120 MHz otherwise the frequencies are: 40 MHz, 80 MHz and 160 MHz. Since the highest clock frequency is obtained directly from the Voltage Controlled Crystal Oscillator (VCXO), different crystals are required for operation in one of the two frequency multiplication modes. A crystal is provided by CERN with each QPLL for operation in the 160MHz mode.

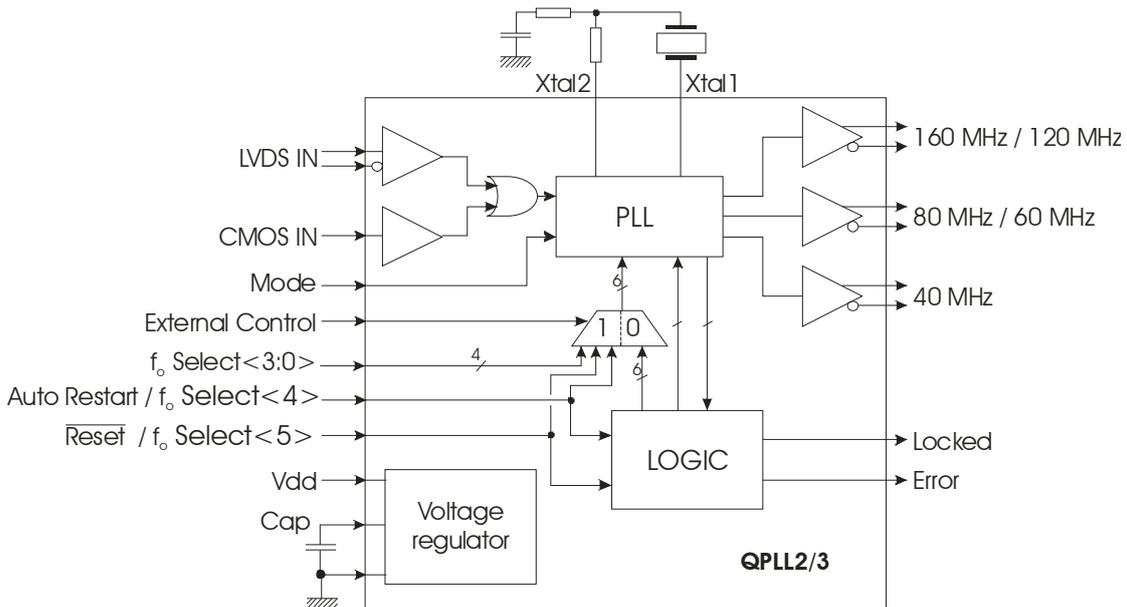


Figure 1 QPLL2 block diagram

The use of a VCXO in the QPLL allows to achieve low jitter figures but imposes the limitation of a small frequency lock range. To cope with crystal cutting accuracy, process, temperature and power supply variations, upon reset or loss of lock, the ASIC goes through a frequency calibration procedure. In principle, this is an automatic procedure that in most applications should be “transparent” to the user. However in some situations, like for example chip or system testing, the user might want to control it. The signals that are relevant to this function are: “externalControl”, “autoRestart” and “f<sub>0</sub>Select<5:0>”. If the “externalControl” signal is set to “1” then the automatic calibration procedure is disabled and the VCXO centre frequency is set by the signals “f<sub>0</sub>Select<5:0>” otherwise, the free running VCXO frequency is automatically determined. Please note that when the “externalControl” signal is set to “1” the signals “autoRestart” and “~reset” become f<sub>0</sub>Select<4> and f<sub>0</sub>Select<5> respectively.

The QPLL contains a lock detection circuit that monitors the lock state of the phase-locked loop. If the PLL is detected to be unlocked, a frequency calibration cycle is initiated to lock the PLL. This feature can be disabled by forcing the signal “autoRestart” to “0”. In this case, a frequency calibration cycle is only started if a reset is applied to the IC. When “externalControl” is forced to “0” the “locked” signal reports the locked status of the PLL. In this case, the lock detection logic filters the random behaviour of the (internal) PLL lock indication. However, if the “externalControl” signal is set to “1” the “Locked” signal will have a random behaviour during loss-of-lock and lock-acquisition.

The logic circuits controlling the PLL use redundant logic techniques to cope with Single Event Upsets (SEU). The “error” flag indicates (momentarily) that one SEU has occurred. These errors are dealt with automatically requiring no action from the user.

## QPLL operation modes

The QPLL operation modes are controlled by the state of the signals “externalControl” and “autoRestart” as indicated on Table 1.

externalControl	autoRestart	Mode
0	0	0
0	1	1
1	x	2

Table 1 QPLL operation mode selection

### Mode 0:

In this mode the QPLL frequency calibration logic is active but a frequency calibration cycle is only executed after a reset.

Mode advantages: Once a first frequency calibration cycle has been executed (with the reference clock present) the QPLL will keep the frequency calibration settings until another reset is applied. This allows the QPLL to acquire lock relatively fast (~250  $\mu$ s) when compared with “mode 1” where a frequency calibration is executed every time lock is lost (~180 ms). This mode can be particularly useful in radiation environments where both the reference clock and the QPLL analogue circuits can be subject to single event upsets.

Mode disadvantages: Because the frequency calibration settings are maintained during operation, only the QPLL analogue range is available to cope with the reference clock drifts and changes in the power supply voltage and temperature (please see Figure 2 for clarification of the terms used). In mode 0, the system where the PLL is integrated must guaranty that the QPLL lock signal is constantly monitored. In the case of loss of lock and if the QPLL does not regain lock after a pre-established delay a reset must be applied so that a new calibration cycle is executed.

### Mode 1:

In this mode the QPLL frequency calibration logic is active, a frequency calibration cycle is executed after a reset or each time lock is lost.

Mode advantages: This mode requires minimum monitoring from the system in where the QPLL is integrated. The QPLL constantly monitors its lock state and executes a frequency calibration cycle every time loss-of-lock is detected. This mode displays the largest tracking range in relation to the reference frequency drifts and the largest tolerance to power supply and temperature variations.

Mode disadvantages: In principle, this should be the preferred mode of operation. However in radiation environments this mode can lead to relatively large “dead times” (~180 ms) since a calibration cycle will be executed each time the reference clock or the analogue circuitry of the QPLL will be disturbed by a single event upset. In those circumstances “mode 0” might be preferable.

### Mode 2:

In this mode the QPLL frequency calibration logic is inactive. The QPLL can be used as a PLL or as a standalone clock generator:

#### Operation as a PLL:

The user must centre the VCXO operation range around the reference clock frequency by setting the bits  $f_0\text{Select}\langle 5:0 \rangle$ . As shown in Figure 2 the settings should be such that the centre of the analogue range is as close as possible to the operation frequency.

Mode advantages: None. Mode mainly used for chip characterization and production testing.

Mode disadvantages: Requires the user to constantly keep track of any changes of circuit characteristics (for example crystal aging) and operation conditions like power supply voltage and temperature.

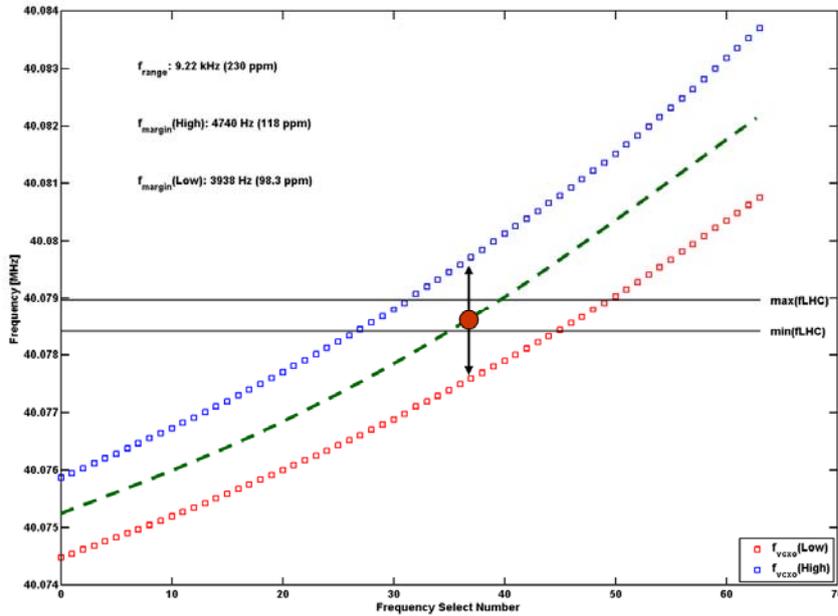


Figure 2. VCXO frequency as function of the digital control bits ( $f_0\text{Select}\langle 5:0 \rangle$ )<sup>1</sup>.

#### Operation as a Clock Source

The QPLL can be used as a standalone crystal oscillator whose frequency can be tuned by the control bits  $f_0\text{Select}\langle 5:0 \rangle$ . In this case the QPLL is simply operated without a reference clock.

In this mode, the clock input can be used as an “extra frequency select bit”. That is, after a given range is selected by the bits  $f_0\text{Select}\langle 5:0 \rangle$  (see Figure 2), the clock input can be used to choose between the maximum and minimum oscillation frequencies of that range. Setting the clock input to a “1” selects the maximum frequency while setting it to “0” selects the minimum frequency.

<sup>1</sup> This picture will be updated once the final quartz crystals will be available. It is used here only as an example. The frequency range is not the target range.

Warning: Mode 1 should never be used for standalone operation (QPLL as a simple clock generator). In that mode and in the absence of a reference clock, the QPLL is constantly executing frequency calibration cycles and its clock outputs are constantly having frequency “jumps”. Any QPLL trying to lock to such a signal will never achieve a stable lock. Mode 2 is thus the only mode recommended to implement a standalone clock source using a QPLL.

## QPLL Signals

**autoRestart** – 5V compatible CMOS input with internal pull-up resistor. The functionality of this signal depends on the state of the “*externalControl*” signal:

**if externalControl = “0”**

*autoRestart* = “0”: Automatic restart of the PLL is disabled. A frequency calibration cycle will only occur after a reset.

*autoRestart* = “1”: Automatic restart is enabled. A frequency calibration cycle will occur each time the PLL is detected to be unlocked or after a reset.

**if externalControl = “1”**

“*autoRestart*” becomes “*f<sub>o</sub>Select<4>*”.

**cap** – VCXO decoupling node:

A 100 nF capacitor must be connected between this pin and ground. Inductance of the interconnection must be minimized.

**error** – 2.5V CMOS output:

This signal indicates that an SEU has occurred. Since SEU events are dealt with automatically by the ASIC logic, this signal will be active only during the period in which the error condition will persist. A SEU on the QPLL logic circuits will not affect the operation of the PLL.

**externalControl** – 5V compatible CMOS input with internal pull-down resistor:

*externalControl* = “0”: The VCXO centre frequency is set by the automatic frequency calibration procedure.

*externalControl* = “1”: The VCXO free running frequency is set by the input signals *f<sub>o</sub>Select<5:0>*.

**f<sub>o</sub>Select<3:0>** - 5V compatible CMOS inputs with internal pull-down/pull-up resistors (*f<sub>o</sub>Select<3>* ← pull-up, *f<sub>o</sub>Select<2>* ← pull-down, *f<sub>o</sub>Select<1>* ← pull-down, *f<sub>o</sub>Select<0>* ← pull-down):

These signals (including *f<sub>o</sub>Select<5:4>*) control the VCXO free running oscillation frequency when the signal “*externalControl*” is set to “1”. If “*externalControl*” is set to “0” these signals have no influence on the IC operation.

**inCMOS** – 5V compatible CMOS clock input with internal pull-down resistor:

This is the CMOS reference clock input. **When in use, “*inLVDS+*” and “*inLVDS-*” must be set to logic levels “0” and “1” respectively.**

**inLVDS+ and inLVDS-** – LVDS clock inputs:

These signals are the LVDS reference clock inputs. **When in use, “*inCMOS*” must be held at logic level “0”.**

**locked** – 2.5V CMOS output:

This signal reports the PLL locked status.

**if externalControl = “0”**

In this case the lock indication is filtered by the QPLL lock detection logic, giving a stable indication during loss-of-lock, lock-acquisition or during lock.

**if externalControl = “1”**

In this case the lock indication state reflects the instantaneous lock indication provided by the PLL. The signal will display a random behaviour during loss-of-lock or lock-acquisition.

**Lvds40MHz+ Ivds40MHz-** – LVDS output:

40MHz clock output

**Ivds80MHz+ Ivds80MHz-** – LVDS output:

*mode* = "0": 60 MHz clock signal (with 120 MHz quartz crystal).

*mode* = "1": 80 MHz clock signal (with 160 MHz quartz crystal).

**Ivds160MHz+ Ivds160MHz-** – LVDS output.

*mode* = "0": 120 MHz clock signal (with 120 MHz quartz crystal).

*mode* = "1": 160 MHz clock (with 160 MHz quartz crystal).

**mode** – 5V compatible CMOS input with internal pull-up resistor:

*mode* = "0": 120 MHz frequency multiplication mode (120 MHz quartz crystal required).

*mode* = "1": 160 MHz frequency multiplication mode (160 MHz quartz crystal required).

**~reset** – 5V compatible CMOS input:

**if externalControl = "0"**

Active low reset signal. It initiates a frequency calibration cycle and lock acquisition.

**if externalControl = "1"**

"~reset" becomes "*f<sub>o</sub>Select<5>*".

**xtal1, xtal2** – Quartz crystal connections pins

## Timing

The QPLL timing diagram is illustrated in Figure 1. The values for the several clock outputs are given in Table 2 and Table 3.

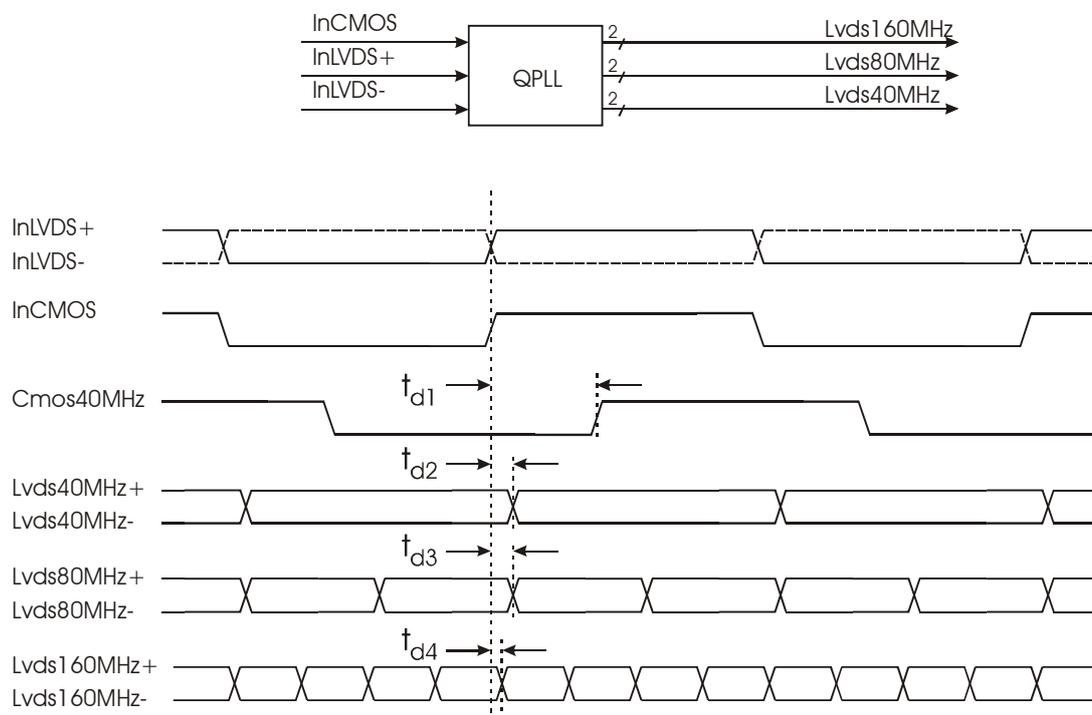


Figure 3 QPLL timing definitions

### CMOS clock reference input

	Min [ns]	Typical [ns]	Max [ns]
$t_{d1}$	1.2	1.6	2.5
$t_{d2}$	1.3	1.7	2.6
$t_{d3}$	1.3	1.7	2.6
$t_{d4}$	0.8	1.2	2.1

Table 2 Output delays referenced to the CMOS clock input

### LVS clock reference input

	Min [ns]	Typical [ns]	Max [ns]
$t_{d1}$	1.1	1.7	3.0
$t_{d2}$	1.2	1.8	3.1
$t_{d3}$	1.2	1.8	3.1
$t_{d4}$	0.7	1.3	2.6

Table 3 Output delays referenced to the LVDS clock input

## QPLL PINOUT

The QPLL is packaged in a 28-pin 5 mm × 5 mm Leadless Plastic Chip Carrier (LPCC-28) with 0.5 mm pin pitch. Additional package information can be obtained from the “ASAT” web site (<http://www.asat.com>).

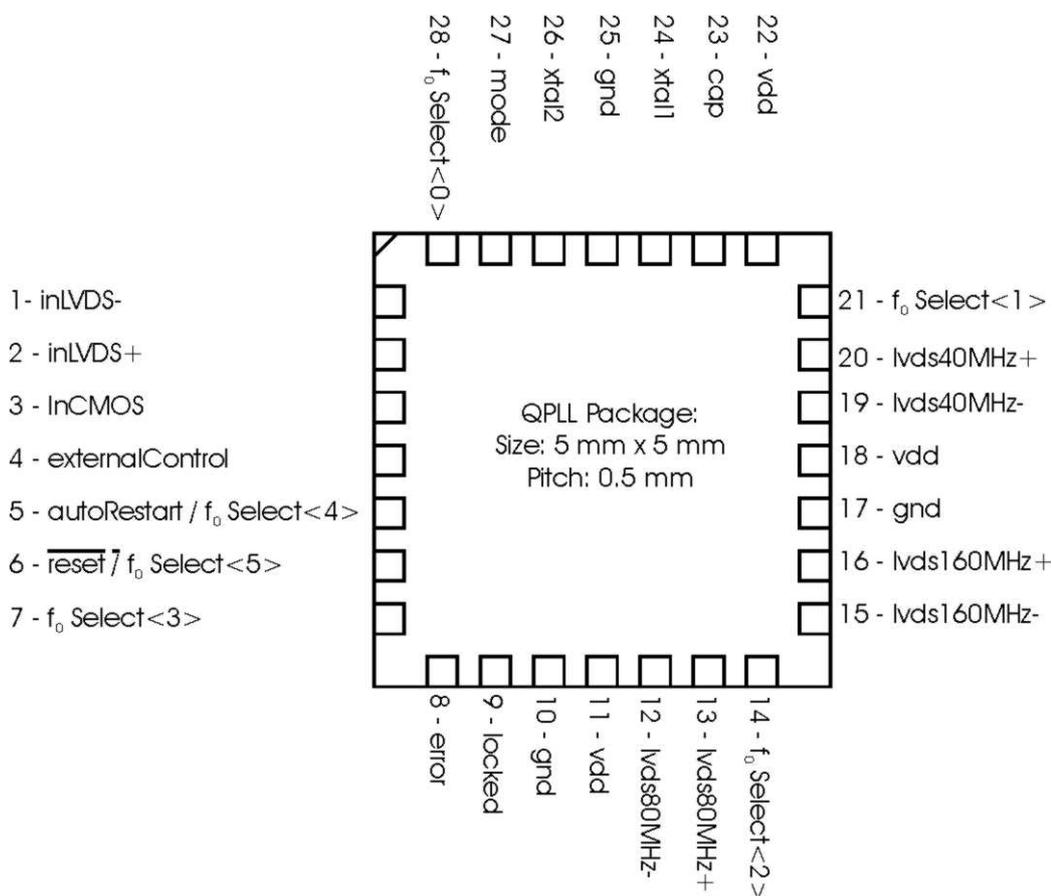


Figure 4 QPLL2 pinout

## Pin assignments

Pin Number	Signal Name	Signal type
1	inLVDS-	Input, LVDS
2	inLVDS+	Input, LVDS
3	inCMOS	Input, CMOS 5V compatible
4	externalControl	Input, CMOS 5V compatible
5	autoRestart / f <sub>0</sub> Select<4>	Input, CMOS 5V compatible
6	~reset / f <sub>0</sub> Select<5>	Input, CMOS 5V compatible
7	f <sub>0</sub> Select<3>	Input, CMOS 5V compatible
8	error	Output, 2.5 V compatible
9	locked	Output, CMOS 2.5 V

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10	gnd	Power
11	vdd	Power
12	lvds80MHz-	Output, LVDS
13	lvds80MHz+	Output, LVDS
14	f <sub>0</sub> Select<2>	Input, CMOS 5V compatible
15	lvds160MHz-	Output, LVDS
16	lvds160MHz+	Output, LVDS
17	gnd	Power
18	vdd	Power
19	lvds40MHz-	Output, LVDS
20	lvds40MHz+	Output, LVDS
21	f <sub>0</sub> Select<1>	Input, CMOS 5V compatible
22	vdd	Power
23	cap	Power
24	xtal1	Analogue, Quartz crystal
25	gnd	power
26	xtal2	Analogue, Quartz crystal
27	mode	Input, CMOS 5V compatible
28	f <sub>0</sub> Select<0>	Input, CMOS 5V compatible

## CRYSTAL SPECIFICATION

A quartz crystal will be provided with each QPLL. The main characteristics of the crystal are given on the following table.

Pos	Description	Symbol	Typ.	Min.	Max.	Unit
1	Crystal type	Inverted mesa AT-Cut				
2	Resonance mode	Fundamental				
3	Load Frequency <sup>3</sup>	<b>FL</b>	160.314744			MHz
4	Load Capacitance	<b>CL</b>	5.5			pF
5	Frequency Tolerance at 25°C	<b>ΔFL/FL</b>		-18	18	ppm
6	Motional Capacitance	<b>C1</b>		4.2		fF
7	Static Capacitance	<b>Co</b>	2.8			pF
8	Drive Level	<b>P</b>			500	μW
9	Operating Temperature Range	<b>OTR</b>		0	60	°C
10	Series Resistance at 25°C	<b>Rs</b>			25	Ohm
11	Drift over OTR	<b>ΔFL/FL</b>		-10	10	ppm
12	Aging first year	<b>ΔFL/FL</b>			± 3	ppm
13	Package type	SMD ceramic				
14	Package surface				29.6	mm <sup>2</sup>
15	Package height				1.75	Mm

Table 4 Quartz crystal specification

<sup>3</sup> This spec needs a 100% frequency verification over temperature range (5 °C intervals)

## POWER REDUCTION NETWORK

### QPLL excess jitter

It was observed that, depending on the operating temperature, the QPLL was generating at some frequencies within the locking range amounts of jitter well above the specification. The problem was investigated by CERN, NEVIS and Micro Crystal (the quartz crystal manufacturer) and it was established that the large jitter behaviour could be explained by activity dips in the crystal. Not all the crystals manufactured reveal the presence of activity dips but it turns out that they appear due to overdrive. The problem is solved by reducing the power delivered to the crystal by inserting an RC network between the QPLL and the crystal as discussed below.

### Recommended network:

The network that should be used to reduce the power delivered to the crystal by the QPLL is represented in Figure 5. It is composed of two resistors (R1 and R2) and a capacitor (C). It should be inserted between the crystal and the QPLL as indicated. Notice that although the crystal is a symmetrical device the network must be connected to pin XTAL2.

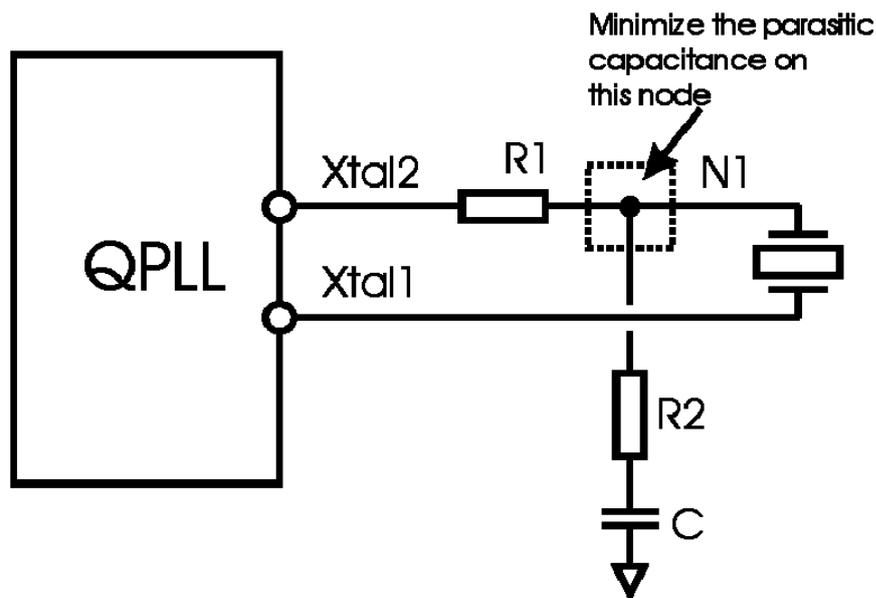


Figure 5 Power reduction network

Values for the circuit components are given on Table 5. If these values are used the QPLL performance remains basically unchanged in what concerns centre frequency, jitter performance and locking range. However, as explained in section "PCB Layout recommendations", to guarantee this some careful layout is mandatory.

Table 5 Component values for the power reduction network

R1 [Ω]	R2 [Ω]	C [nF]
62	240	10

It is not possible to predict which crystals will display activity dips so it is absolutely recommended the use of this network. Values in Table 5 must be respected.

## POWER SUPPLY SENSITIVITY

Some of the QPLL characteristics are power supply voltage dependent: namely the VCXO free-running oscillation frequency and the static phase error. Both of these variables have an influence on the jitter performance. It is thus advisable to keep the noise levels on the power supply to the minimum possible. The numbers given below will help the user to form an opinion on how much noise can be tolerated on the power supply without incurring performance degradation.

### Static phase error

The PLL, inside the QPLL ASIC, is a control loop that tries to maintain zero phase error between the reference clock and the internally generated VCXO clock. However, both these clocks propagate through clock buffers that introduce a non-zero delay between the two signals (see Timing). More over, since these buffers are external to the PLL control loop their power supply dependence is not compensated for. Variations in the power supply will result thus in a varying phase delay between the two clock signals.

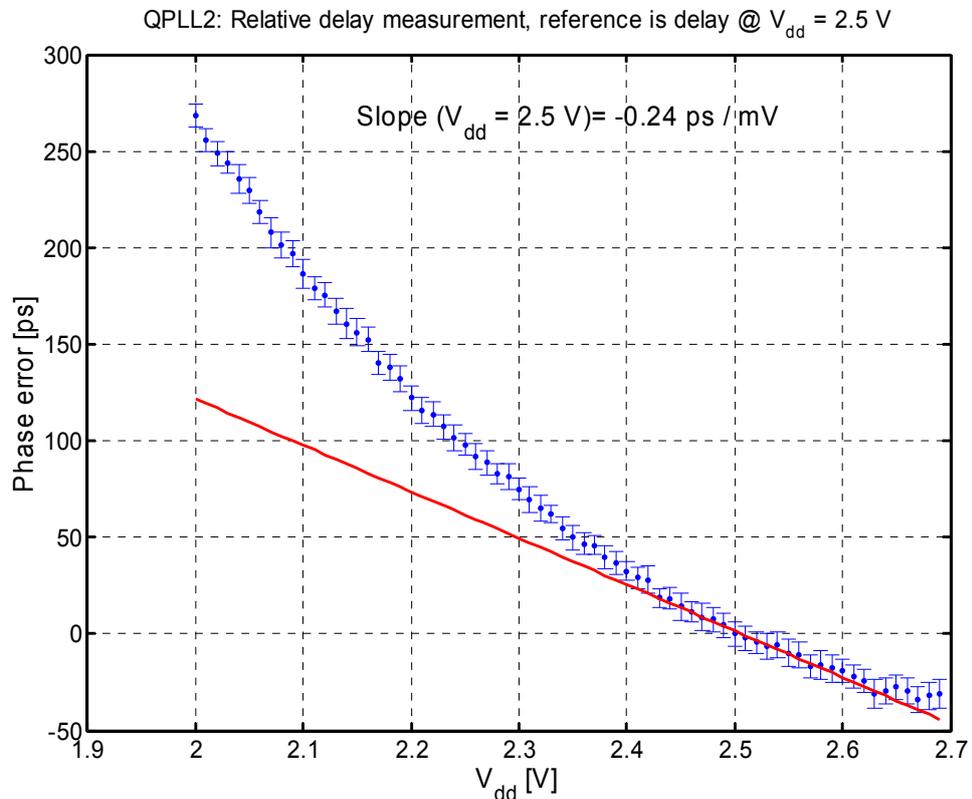


Figure 6 Phase error as function of the power supply voltage (relative measurement). In this measurement the reference clock is fed to the CMOS input

Figure 6 displays a typical curve for the static phase error as a function of the power supply voltage. In this case, the CMOS clock input is used as the clock reference input. The measurement is relative, that is, the phase error introduced by varying the power supply is measured relative to the static phase error when the power supply voltage is 2.5 V (the nominal power supply voltage). The curve displays a slope of  $-0.24$  ps/mV at 2.5 V. Similarly, Figure 7 displays the static phase error when the LVDS input is used. In this case the slope of the curve is  $-0.72$  ps/mV for the nominal power supply voltage.

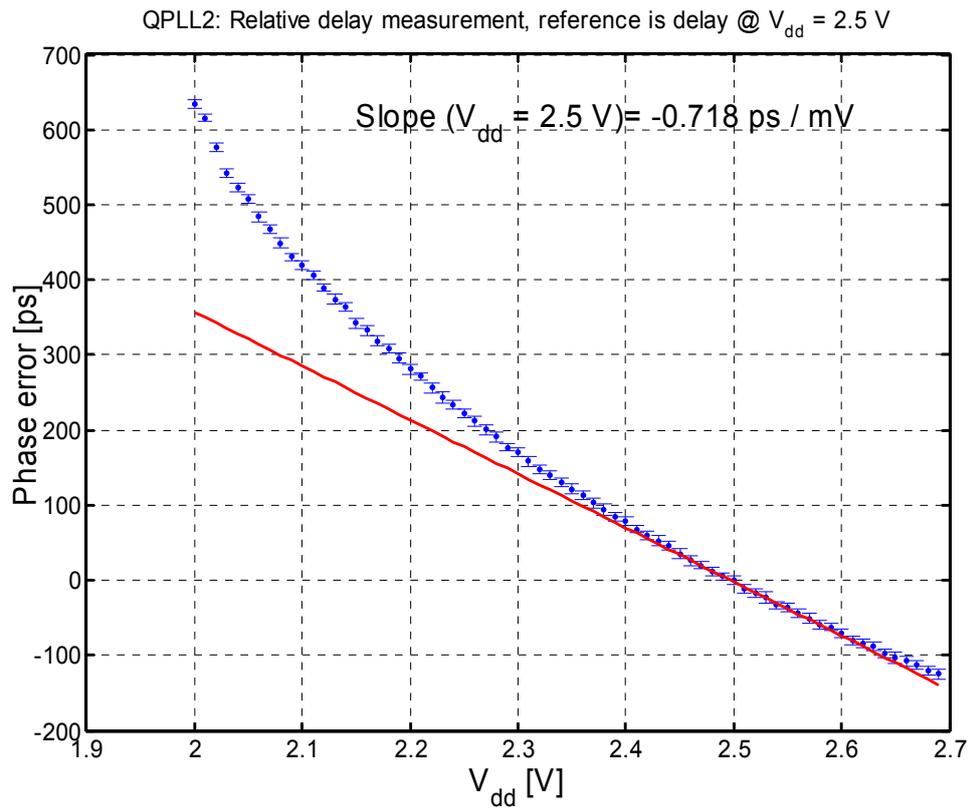


Figure 7 Phase error as function of the power supply voltage (relative measurement). In this measurement the reference clock is fed to the LVDS input.

## VCXO free-running oscillation frequency

The QPLL can run stand alone as a clock source (see Operation as a Clock Source). When running in this mode there is no external reference to be tracked and the VCXO will produce a frequency which is essentially dependent on the quartz crystal being used and on the ASIC settings chosen. However, since no reference signal is being tracked, the power supply voltage will have some influence on the oscillator frequency.

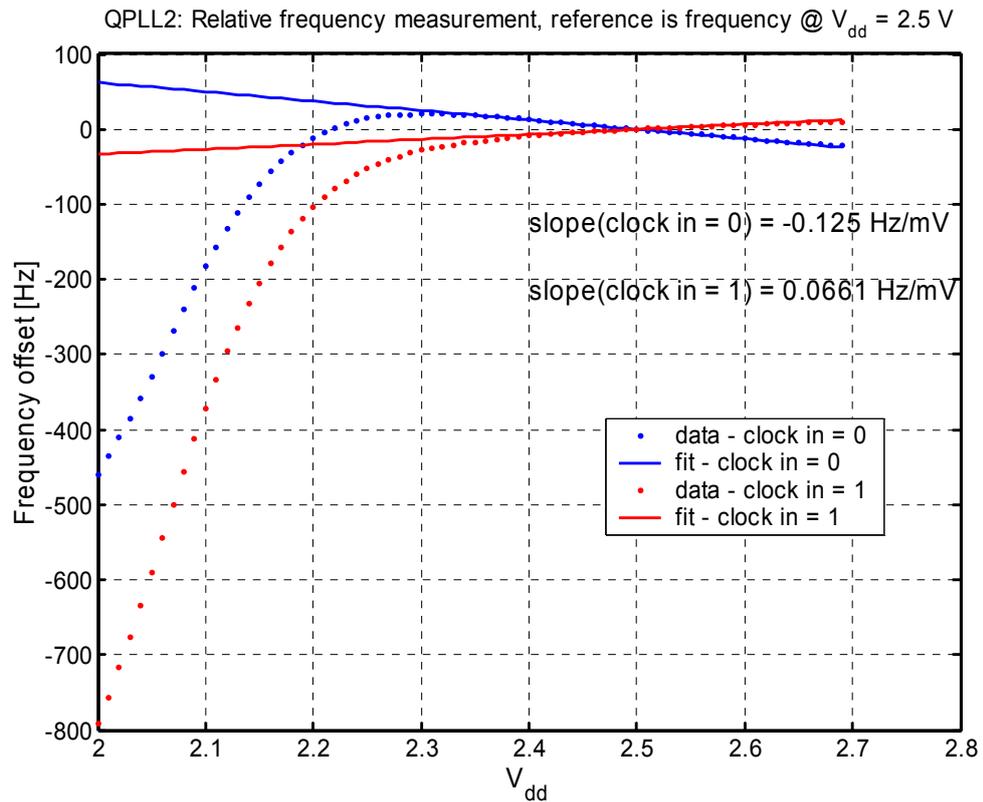


Figure 8 VCXO Oscillation frequency as function of the power supply voltage (relative measurement)

Figure 8 displays the VCXO oscillation frequency offset as function of the power supply voltage. The measurements are made relative to the VCXO frequency when the power supply voltage is 2.5 V. Notice that two curves are plotted: one corresponding to the reference clock in put set to “0” and the other one with the input set to “1”. In absolute value the slopes of both curves are less than 0.13 Hz/mV at  $V_{dd} = 2.5\text{ V}$ . Notice that the dependence on the power supply increases once the ASIC is powered with a voltage smaller than 2.3 V. Such a regime of operation should be avoided. In other to keep some operation margin it is recommended that the minimum power supply voltage should not be reduced below 2.4 V. This is valid for operation both in the PLL mode and on the Clock Source mode.

## PCB LAYOUT RECOMMENDATIONS

### Frequency pulling considerations

The QPLL is based on a Voltage Controlled Quartz Crystal Oscillator (VCXO). The frequency of oscillation of such circuit is essentially imposed by the quartz crystal resonance frequency. However, the circuit capacitance (which includes the layout parasitics) will also have an influence. In the case of a VCXO, this manifests itself in two ways: first, the oscillation frequency is not exactly the quartz crystal resonance frequency but higher (called the *loaded oscillation frequency*) and second, the frequency pulling capability of the circuit is affected by the total circuit capacitance, in particular by the minimum capacitance achievable.

To cope with any frequency uncertainty the crystal is specified for a given load capacitance. This gives the manufacturer the capability of tuning the crystal to a specific circuit.

Concerning the pulling range, one could be tempted to think that adding as much variable capacitance as possible would be a solution to increase the frequency pulling ability of the circuit. However, in the limit of an infinite load capacitance the oscillation frequency tends to the crystal resonance frequency. In this limit, the frequency sensitivity to capacitance variations is very small and the VCXO has thus a small pulling ability<sup>4</sup>. The solution is thus to work on the extreme of low capacitances where the frequency sensitivity is maximised. Figure 9 illustrates these concepts for a practical crystal (in this figure C12 represents the crystal package capacitance).

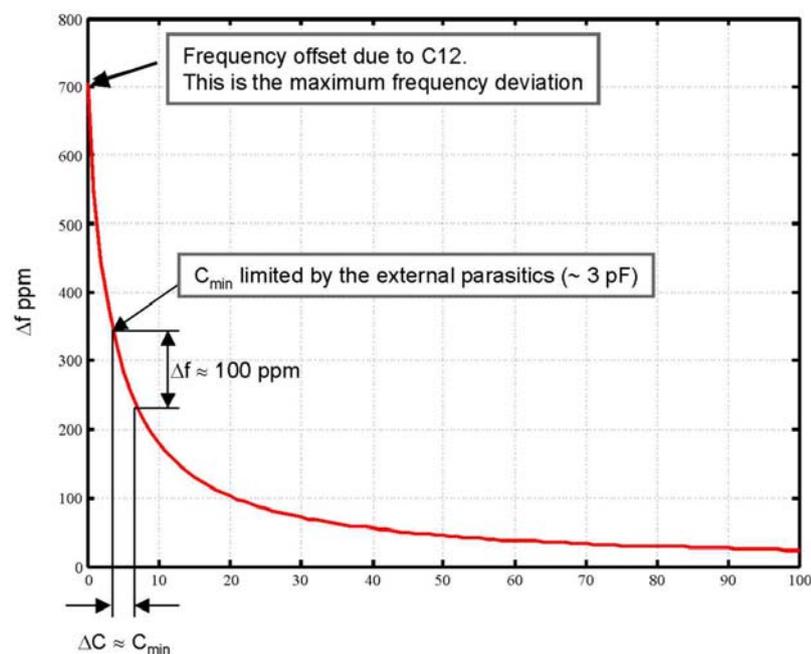


Figure 9 Circuit capacitance versus frequency pulling ability

We are thus faced with two problems: first, minimise the parasitic capacitances introduced by the circuit layout so that the pulling range does not get degraded and

<sup>4</sup> This would be a good solution if the capacitance could be strictly varied from a very small to a large value. However, in practical circuits a large maximum value also implies a relatively large minimum value. That is, the ratio between the minimum and maximum capacitance cannot be freely chosen.

second, make sure that the circuits built by the QPLL users display a load capacitance which is identical to the specified crystal load capacitance. It is thus strongly recommended that the users adopt the layout represented in Figure 10 for the interconnections between the QPLL and the quartz crystal. Failing to do so, it might result in the best case in a reduced or asymmetrical lock range and in the worst case in the impossibility to lock to the LHC frequency. It is thus the user responsibility to follow the recommended layout for the interconnections between the quartz crystal and the QPLL as close as possible.

From a simple parallel plate capacitance calculation the interconnection between Xtal1 and the crystal (crystal and IC soldering pads plus the PCB track) contributes a capacitance to ground of about 0.47pF. This value can be used as a guideline to design the PCB. However, in any case the user should check that the QPLL locking range is well centred around the LHC frequency using the procedure described in the following section.

## Layout

As indicated in Figure 5, it is very important to minimize any stray capacitances on node 1 (N1) of the resistive divider. To have an idea of the parasitic capacitances in the circuit, just the crystal soldering pad alone represents about 0.43 pF if the dielectric has a thickness of 800 μm (0.49 pF for 700 μm and 1.72 pF for 200 μm). The parasitic capacitance on node N1 has two detrimental effects: First, it increases the power delivered to the crystal, and second it pulls low the resonance frequency of the circuit. It is thus important to reduce as much as possible the parasitic capacitance on this node. For that, the power and ground planes should be eliminated under the soldering pads of R1, R2 and the crystal soldering pad that is connected to this node. Signal routing must be avoided under this area. Please see Figure 10 for a suggestion on how the layout should be done.

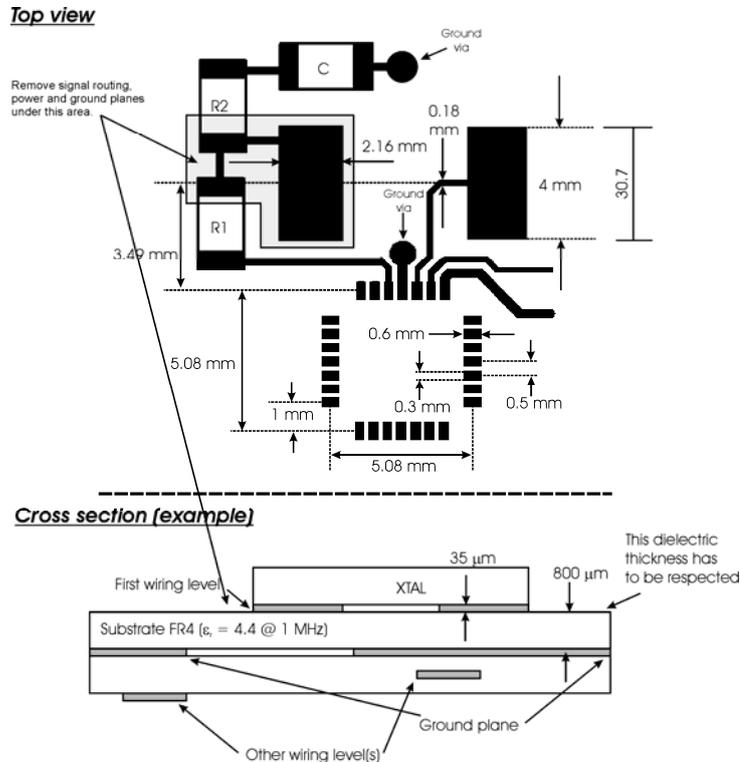


Figure 10 Recommend layout for the QPLL and crystal interconnection

To facilitate the CAD work a schematic capture symbol and the layout footprint of the ASIC are available in the CERN CADENCE library. The footprint is available in the

library CNSPECIAL under the name QPLL. For the package type the LPCC option must be used.

As an example of a QPLL circuit the designer can refer to the TTCrq schematics and layout files. Links to these files can be found on the QPLL web site: <http://www.cern.ch/proj-qpll>.

## Procedure to verify the PCB parasitic capacitance

There are two alternative ways to verify that the PCB has been correctly designed:

The first (and simplest) is to check the circuit lock range. This can be done by sweeping the input frequency around the LHC frequency. By approaching the LHC frequency from below the lower locking frequency can be obtained. Similarly, by approaching the LHC frequency from above the upper locking frequency can be determined. The LHC frequency ( $f_{LHC}$ ) must be well centred within these two limits. For these measurements the frequency sweep should be done in “digital” steps allowing, at each frequency step, time enough for a calibration cycle to be executed.

The second method consists in measuring the free running oscillation frequency of the PLL. The following procedure needs to be applied: set the signal “*externalControl*” to “1” and the signals “*f<sub>o</sub>Select<5:0>*” to “100111”<sup>1</sup> (binary). Then, measure the output frequency while the reference clock input is forced to “0”. This will give the minimum oscillation frequency ( $f_{o[min]}$ ) for the selected frequency range. Then repeat the measurement forcing the reference clock input to “1”. This will give  $f_{o[max]}$  for that range. The average of these two frequencies ( $f_{o[min]}$  and  $f_{o[max]}$ ) must be within:  $f_{LHC} \pm 25$  ppm.

Please note all the frequency measurements mentioned above need to be done with an absolute accuracy of at least a few parts per million (ppm). Although most laboratory frequency meters are capable of providing such relative accuracy they are rarely that accurate in absolute terms. The solution in that case is to feed the frequency meter with a precise clock signal from a calibrated frequency standard (like for example a GPS based frequency source).

At CERN we are equipped to do such precise frequency measurements and we can help users that aren’t equipped to do so in their own labs.

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<sup>1</sup> Number to be confirmed once the crystals will be received from the manufacturer.