QPLL Measurements

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Crystals

Micro crystal kindly provided five crystals cut to 160.314744 MHz (approximately four times the LHC nominal frequency - see VCXO report for details). These crystal were used both in the characterization of the QPLL ASIC as well as in data transmission tests done using the GOL, the QPLL and the TTCrx. The principal characteristics of these devices are given in Table 1.

Crystal #	Resonance frequency [MHz]	Motional resistance [Ω]	Motional Capacitance [fF]	Shunt capacitance [pF]
1	160.236739	8.4	6.20	2.54
2	160.241742	9.2	5.94	2.53
3	160.242429	9.3	5.78	2.56
4	160.243251	8.8	5.65	2.52
5	160.241056	8.7	5.79	2.53

Table 1 Crystals main characteristics

The above crystals when loaded with a 3.75 pF equivalent capacitance oscillator should produce the desired frequency (160.314744 MHz = 4 × 40.078686 MHz) within ± 18 ppm. The estimated load capacitance was obtained from previous measurements of the VCXO and the expected package and layout parasitics. It turned out that the load capacitance was under estimated by 0.72 pF (in average). However, even in these conditions, it was always possible to pull the QPLL frequency to the nominal LHC value of 40.078686 MHz.

Data transmission tests

One of the main aims of the QPLL development is to allow the use of the TTCrx as a clock source for Gbit/s data links once its clock signal is jitter filtered. To prove this, two tests were done whose basic block diagrams are represented Figure 1

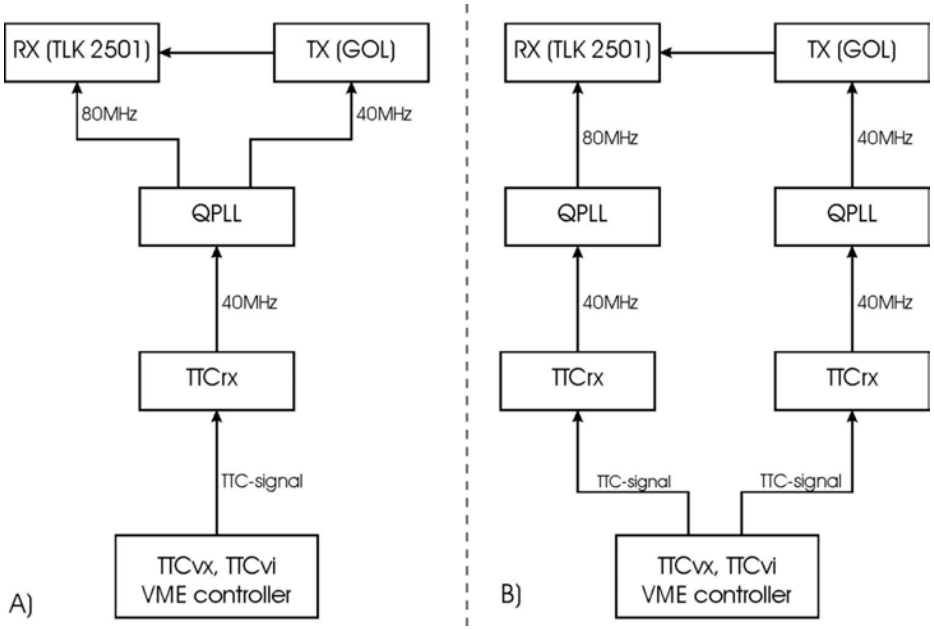

Figure 1 Data transmission test setups

In the first test (Figure 1, A)) a single QPLL was used as the clock source for both the serializer (the GOL) and the deserializer (the TLK 2501). The GOL was clocked with the QPLL 40 MHz clock output while the deserializer was clocked by the 80 MHz output. The QPLL received a clock signal from the TTCrx that was driven by a TTC system composed of the TTCvx, the TTCvi and a VME controller. During the test, both data and triggers were sent over the optical channel (TTC-signal in the figure) being the maximum trigger rate approximately 400 KHz (limited by the test setup). The test was run continuously at 1.6 Gbit/s during three days without any transmission errors.

A second test was done in conditions similar to the previous one but, as represented in Figure 1 B), in that case two QPLL's and two TTCrx's were used to provide independent cocks to the transmitter and receiver. The test was run continuously at 1.6 Gbit/s during one week without any transmission error.

QPLL characterization – Chip on PCB

A QPLL was characterized using the five crystals provided by Micro Crystal. To do the tests, a QPLL was soldered to the QPLL test fixture (see Test Fixture) and the crystals were put in electrically contact with the circuit by maintaining them under mechanical pressure against the PCB. A signal generator with 10 Hz resolution was used as the clock source and the Agilent 53132A universal counter was used to measure the frequency with 1Hz accuracy. No attempt was made to frequency calibrate the universal counter however, this instrument was a recent acquisition and it was factory calibrated.

Table 1 summarizes the test results for this measurement (see Detailed data for "Chip on PCB" for more detailed numbers). As can be seen from the table the PLL lock range is in average 5.8 kHz (146 ppm). The average value of the frequency[1] offset is –41 ppm while the design target was a frequency error smaller than 25 ppm in absolute value (if crystal cutting accuracy and circuit tolerances are taken into account). As, discussed before, this frequency error was due to under estimation of the loading capacitance represented by the oscillator plus the package and PCB routing. The measurements reveal an average loading capacitance of 4.47 pF while the crystal cutting was specified for 3.75 pF loading.

Crystal	f_{center} [MHz]	f_{offset} [kHz]	$C_{circuit}$ [pF]	Digital Range [kHz]	<Analog Range> [kHz]	f_{lock} (min) [MHz]	f_{lock} (max) [MHz]	Lock Range [kHz]
1	40.076958	-1.728 (-43 ppm)	4.45	3.422 (85 ppm)	2.873 (72 ppm)	40.074163	40.080523	6.360 (159 ppm)
2	40.077590	-1.095 (-27 ppm)	4.40	3.244 (81)	2.717 (68)	40.074933	40.080973	6.040 (150 ppm)
3	40.077060	-1.626 (-41 ppm)	4.48	3.119 (78 ppm)	2.627 (66 ppm)	40.074534	40.080344	5.810 (145 ppm)
4	40.076946	-1.740 (-43 ppm)	4.49	2.985 (74 ppm)	2.488 (62 ppm)	40.074516	40.080087	5.571 (139 pp)
5	40.076633	-2.053 (-51 ppm)	4.55	2.944 (74 ppm)	2.464 (62 ppm)	40.074237	40.079727	5.490 (137 ppm)

Table 2 Measurement results summary for "chip on board" (see Detailed data for "Chip on PCB")

QPLL characterization – Chip on Test Socket

Twenty QPLL's were also measured together with crystal "1" to assess the variability introduced by the ASIC. The same procedure as above was adopted but, in this case, the chips were assembled in a test socket to allow easy interchange of devices. As can be seen from the numbers in Table 3 the additional parasitic capacitance introduced by the test socket result in a larger frequency offset (in absolute value) and a shorter lock range as expected.

[1] In Table 2 frequency offset (f_{offset}) is the difference between the target frequency 40.078686 MHz and the center frequency (f_{center}) of the analog range of the VCXO when the digital control is set to "1000".

Chip Number	f_{lock} (min) [MHz]	f_{lock} (max) [MHz]	f_{center} [MHz]	f_{offset} [KHz]	f_{offset} [ppm]	Lock range [KHz]	Lock range [ppm]	Phase (relative) [ps]	Equivalent Capacitance [pF]
1	40.072934	40.078414	40.075674	-3.012	-75	5.480	137	reference	4.99
2	40.072967	40.078458	40.075712	-2.974	-74	5.491	137	0	4.97
3	40.072969	40.078449	40.075709	-2.977	-74	5.480	137	-120	4.97
4	40.072970	40.078460	40.075715	-2.971	-74	5.490	137	-121	4.97
5	40.072991	40.078462	40.075727	-2.959	-74	5.471	137	-18	4.97
6	40.072973	40.078443	40.075708	-2.978	-74	5.470	136	-18	4.97
7	40.072925	40.078426	40.075676	-3.010	-75	5.501	137	-2	4.99
8	40.072966	40.078446	40.075706	-2.980	-74	5.480	137	0	4.98
9	40.072957	40.078427	40.075692	-2.994	-75	5.470	136	-106	4.98
10	40.072958	40.078458	40.075708	-2.978	-74	5.500	137	-85	4.97
11	40.072969	40.078440	40.075705	-2.981	-74	5.471	137	27	4.98
12	40.072991	40.078481	40.075736	-2.950	-74	5.490	137	-17	4.96
13	40.073002	40.078501	40.075752	-2.934	-73	5.499	137	27	4.95
14	40.072973	40.078453	40.075713	-2.973	-74	5.480	137	40	4.97
15	40.072974	40.078454	40.075714	-2.972	-74	5.480	137	58	4.97
16	40.072955	40.078435	40.075695	-2.991	-75	5.480	137	11	4.98
17	40.072976	40.078446	40.075711	-2.975	-74	5.470	136	21	4.97
18	40.072996	40.078486	40.075741	-2.945	-73	5.490	137	46	4.96
19	40.072996	40.078456	40.075726	-2.960	-74	5.460	136	-142	4.97
20	40.072966	40.078436	40.075701	-2.985	-74	5.470	136	-156	4.98
< >	40.072970 MHz	40.078452 MHz	40.075711 MHz	-2.975 KHz	-74 ppm	5.481 KHz	137 ppm	-27.8 ps	4.97 pF
σ	20 Hz	21 Hz	10 Hz	19 Hz	0.5 ppm	12 Hz	0.3 ppm	68 ps	9 fF
P-P	77 Hz	87 Hz	77 Hz	77 Hz	2 ppm	41 Hz	1 ppm	214 ps	35 fF

Table 3 Measurement results for "Chip on Test Socket"

The numbers show that the chip contributes less than 77 Hz (2 ppm) to the frequency uncertainty (all ASICs belong to the same production lot). Chips display a very similar locking range. However, it is necessary to take into consideration that parasitic PCB capacitance has an impact on the locking range and that the Crystal motional capacitance is the dominant parameter in determining the locking range.
A relative phase measurement was also made. The phase of chip "1" was taken as the reference and the phase of all the other ASICs was compared with it. As can be seen from the table once locked the phase difference between chips never exceed 214 ps.

Detailed data for "Chip on PCB"

Xtal: 1

Count	f_{min} [MHz]	f_{max} [MHz]	f_{center} [MHz]	f_{offset} [kHz]	f_{offset} [ppm]	$\Delta f_{digital}$ [kHz]	$\Delta f_{digital}$ [ppm]	Δf_{analog} [kHz]	Δf_{analog} [ppm]	$C_{circuit}$ [pF]
0000	40.074147	40.076473	40.075310	-3.376	-84	-	-	2.326	58	5.16
0001	40.074305	40.076689	40.075497	-3.189	-80	0.187	5	2.384	59	5.07
0010	40.074466	40.076911	40.075688	-2.998	-75	0.192	5	2.445	61	4.98
0011	40.074632	40.077140	40.075886	-2.800	-70	0.198	5	2.508	63	4.89
0100	40.074802	40.077367	40.076085	-2.602	-65	0.199	5	2.565	64	4.81
0101	40.074975	40.077609	40.076292	-2.394	-60	0.207	5	2.634	66	4.72
0110	40.075155	40.077861	40.076508	-2.178	-54	0.216	5	2.706	68	4.63
0111	40.075336	40.078122	40.076729	-1.957	-49	0.221	6	2.786	70	4.54
1000	40.075523	40.078393	40.076958	-1.728	-43	0.229	6	2.870	72	4.45
1001	40.075712	40.078669	40.077191	-1.496	-37	0.233	6	2.957	74	4.36
1010	40.075906	40.078954	40.077430	-1.256	-31	0.239	6	3.048	76	4.26
1011	40.076106	40.079248	40.077677	-1.009	-25	0.247	6	3.142	78	4.17
1100	40.076306	40.079540	40.077923	-0.763	-19	0.246	6	3.234	81	4.09
1101	40.076513	40.079854	40.078184	-0.502	-13	0.261	6	3.341	83	3.99
1110	40.076725	40.080180	40.078452	-0.234	-6	0.269	7	3.455	86	3.90
1111	40.076945	40.080519	40.078732	0.046	1	0.280	7	3.574	89	3.81

f_{center} [MHz]	f_{offset} [kHz]	$C_{circuit}$ [pF]	Digital Range [kHz]	<Analog Range> [kHz]	f_{lock} (min) [MHz]	f_{lock} (max) [MHz]	Lock Range [kHz]
40.076958	-1.728 (-43 ppm)	4.45	3.422 (85 ppm)	2.873 (72 ppm)	40.074163	40.080523	6.360 (159 ppm)

Xtal: 2

Count	f_{min} [MHz]	f_{max} [MHz]	f_{center} [MHz]	f_{offset} [kHz]	f_{offset} [ppm]	$\Delta f_{digital}$ [kHz]	$\Delta f_{digital}$ [ppm]	Δf_{analog} [kHz]	Δf_{analog} [ppm]	$C_{circuit}$ [pF]
0000	40.074928	40.077133	40.076031	-2.656	-66	-	-	2.205	55	5.10
0001	40.075078	40.077346	40.076212	-2.474	-62	0.181	5	2.268	57	5.01
0010	40.075231	40.077556	40.076394	-2.293	-57	0.181	5	2.325	58	4.92
0011	40.075389	40.077773	40.076581	-2.105	-53	0.188	5	2.384	59	4.84
0100	40.075548	40.077992	40.076770	-1.916	-48	0.189	5	2.444	61	4.75
0101	40.075712	40.078221	40.076966	-1.720	-43	0.197	5	2.509	63	4.67
0110	40.075882	40.078456	40.077169	-1.517	-38	0.203	5	2.574	64	4.58
0111	40.076056	40.078699	40.077377	-1.309	-33	0.208	5	2.643	66	4.49
1000	40.076235	40.078946	40.077590	-1.095	-27	0.213	5	2.711	68	4.40
1001	40.076417	40.079202	40.077810	-0.876	-22	0.219	5	2.785	69	4.32
1010	40.076601	40.079470	40.078035	-0.650	-16	0.226	6	2.869	72	4.23
1011	40.076788	40.079745	40.078266	-0.419	-10	0.231	6	2.957	74	4.14
1100	40.076980	40.080027	40.078503	-0.183	-5	0.237	6	3.047	76	4.05
1101	40.077183	40.080323	40.078753	0.067	2	0.250	6	3.140	78	3.96
1110	40.077387	40.080634	40.079011	0.325	8	0.258	6	3.247	81	3.87
1111	40.077595	40.080955	40.079275	0.589	15	0.265	7	3.360	84	3.78

f_{center} [MHz]	f_{offset} [kHz]	$C_{circuit}$ [pF]	Digital Range [kHz]	<Analog Range> [kHz]	f_{lock} (min) [MHz]	f_{lock} (max) [MHz]	Lock Range [kHz]
40.077590	-1.095 (-27 ppm)	4.40	3.244 (81)	2.717 (68)	40.074933	40.080973	6.040 (150 ppm)

Xtal: 3

Count	f_{min} [MHz]	f_{max} [MHz]	f_{center} [MHz]	f_{offset} [kHz]	f_{offset} [ppm]	$\Delta f_{digital}$ [kHz]	$\Delta f_{digital}$ [ppm]	Δf_{analog} [kHz]	Δf_{analog} [ppm]	$C_{circuit}$ [pF]
0000	40.074522	40.076619	40.075570	-3.115	-78	-	-	2.097	52	5.18
0001	40.074659	40.076814	40.075736	-2.950	-74	0.166	4	2.155	54	5.09
0010	40.074805	40.077018	40.075911	-2.775	-69	0.175	4	2.213	55	5.00
0011	40.074954	40.077227	40.076090	-2.595	-65	0.179	4	2.273	57	4.92
0100	40.075105	40.077439	40.076272	-2.414	-60	0.181	5	2.334	58	4.83
0101	40.075259	40.077660	40.076459	-2.227	-56	0.188	5	2.401	60	4.74
0110	40.075419	40.077890	40.076654	-2.031	-51	0.195	5	2.471	62	4.65
0111	40.075582	40.078127	40.076855	-1.831	-46	0.200	5	2.545	64	4.56
1000	40.075749	40.078371	40.077060	-1.626	-41	0.205	5	2.622	65	4.48
1001	40.075919	40.078623	40.077271	-1.415	-35	0.211	5	2.704	67	4.39
1010	40.076094	40.078885	40.077489	-1.196	-30	0.219	5	2.791	70	4.30
1011	40.076273	40.079156	40.077714	-0.972	-24	0.225	6	2.883	72	4.21
1100	40.076456	40.079433	40.077945	-0.742	-19	0.230	6	2.977	74	4.12
1101	40.076645	40.079724	40.078184	-0.501	-13	0.240	6	3.079	77	4.03
1110	40.076840	40.080025	40.078432	-0.254	-6	0.248	6	3.185	79	3.93
1111	40.077042	40.080338	40.078690	0.004	0	0.258	6	3.296	82	3.84

f_{center} [MHz]	f_{offset} [kHz]	$C_{circuit}$ [pF]	Digital Range [kHz]	<Analog Range> [kHz]	f_{lock} (min) [MHz]	f_{lock} (max) [MHz]	Lock Range [kHz]
40.077060	-1.626 (-41 ppm)	4.48	3.119 (78 ppm)	2.627 (66 ppm)	40.074534	40.080344	5.810 (145 ppm)

Xtal: 4

Count	f_{min} [MHz]	f_{max} [MHz]	f_{center} [MHz]	f_{offset} [kHz]	f_{offset} [ppm]	$\Delta f_{digital}$ [kHz]	$\Delta f_{digital}$ [ppm]	Δf_{analog} [kHz]	Δf_{analog} [ppm]	$C_{circuit}$ [pF]
0000	40.074496	40.076535	40.075516	-3.171	-79	-	-	2.039	51	5.18
0001	40.074638	40.076716	40.075677	-3.009	-75	0.162	4	2.078	52	5.09
0010	40.074781	40.076908	40.075845	-2.841	-71	0.168	4	2.127	53	5.01
0011	40.074935	40.077102	40.076019	-2.668	-67	0.174	4	2.167	54	4.92
0100	40.075083	40.077302	40.076192	-2.494	-62	0.174	4	2.219	55	4.84
0101	40.075242	40.077508	40.076375	-2.311	-58	0.183	5	2.266	57	4.75
0110	40.075398	40.077725	40.076561	-2.124	-53	0.187	5	2.327	58	4.66
0111	40.075555	40.077945	40.076750	-1.936	-48	0.189	5	2.390	60	4.58
1000	40.075716	40.078176	40.076946	-1.740	-43	0.196	5	2.460	61	4.49
1001	40.075874	40.078412	40.077143	-1.543	-39	0.197	5	2.538	63	4.41
1010	40.076041	40.078660	40.077351	-1.335	-33	0.207	5	2.619	65	4.32
1011	40.076207	40.078917	40.077562	-1.124	-28	0.211	5	2.710	68	4.24
1100	40.076381	40.079183	40.077782	-0.904	-23	0.220	5	2.802	70	4.15
1101	40.076558	40.079464	40.078011	-0.675	-17	0.229	6	2.906	73	4.06
1110	40.076745	40.079757	40.078251	-0.435	-11	0.240	6	3.012	75	3.97
1111	40.076930	40.080071	40.078500	-0.186	-5	0.250	6	3.141	78	3.88

f_{center} [MHz]	f_{offset} [kHz]	$C_{circuit}$ [pF]	Digital Range [kHz]	<Analog Range> [kHz]	f_{lock} (min) [MHz]	f_{lock} (max) [MHz]	Lock Range [kHz]
40.076946	-1.740 (-43 ppm)	4.49	2.985 (74 ppm)	2.488 (62 ppm)	40.074516	40.080087	5.571 (139 pp)

Xtal: 5

Count	f_{min} [MHz]	f_{max} [MHz]	f_{center} [MHz]	f_{offset} [kHz]	f_{offset} [ppm]	$\Delta f_{digital}$ [kHz]	$\Delta f_{digital}$ [ppm]	Δf_{analog} [kHz]	Δf_{analog} [ppm]	$C_{circuit}$ [pF]
0000	40.074225	40.076226	40.075226	-3.461	-86	-	-	2.001	50	5.22
0001	40.074365	40.076401	40.075383	-3.303	-82	0.158	4	2.036	51	5.14
0010	40.074503	40.076591	40.075547	-3.139	-78	0.164	4	2.088	52	5.06
0011	40.074650	40.076788	40.075719	-2.967	-74	0.172	4	2.138	53	4.97
0100	40.074798	40.076988	40.075893	-2.793	-70	0.174	4	2.190	55	4.89
0101	40.074941	40.077192	40.076067	-2.619	-65	0.173	4	2.251	56	4.81
0110	40.075091	40.077410	40.076251	-2.436	-61	0.184	5	2.319	58	4.72
0111	40.075255	40.077633	40.076444	-2.242	-56	0.194	5	2.378	59	4.64
1000	40.075405	40.077861	40.076633	-2.053	-51	0.189	5	2.456	61	4.55
1001	40.075569	40.078098	40.076833	-1.853	-46	0.201	5	2.529	63	4.47
1010	40.075733	40.078342	40.077038	-1.649	-41	0.204	5	2.609	65	4.38
1011	40.075903	40.078595	40.077249	-1.437	-36	0.211	5	2.692	67	4.30
1100	40.076074	40.078855	40.077464	-1.222	-30	0.216	5	2.781	69	4.21
1101	40.076252	40.079128	40.077690	-0.996	-25	0.226	6	2.876	72	4.12
1110	40.076435	40.079418	40.077926	-0.759	-19	0.236	6	2.983	74	4.03
1111	40.076623	40.079716	40.078170	-0.516	-13	0.243	6	3.093	77	3.95

f_{center} [MHz]	f_{offset} [kHz]	$C_{circuit}$ [pF]	Digital Range [kHz]	<Analog Range> [kHz]	f_{lock} (min) [MHz]	f_{lock} (max) [MHz]	Lock Range [kHz]
40.076633	-2.053 (-51 ppm)	4.55	2.944 (74 ppm)	2.464 (62 ppm)	40.074237	40.079727	5.490 (137 ppm)