News on VCO for QPLL

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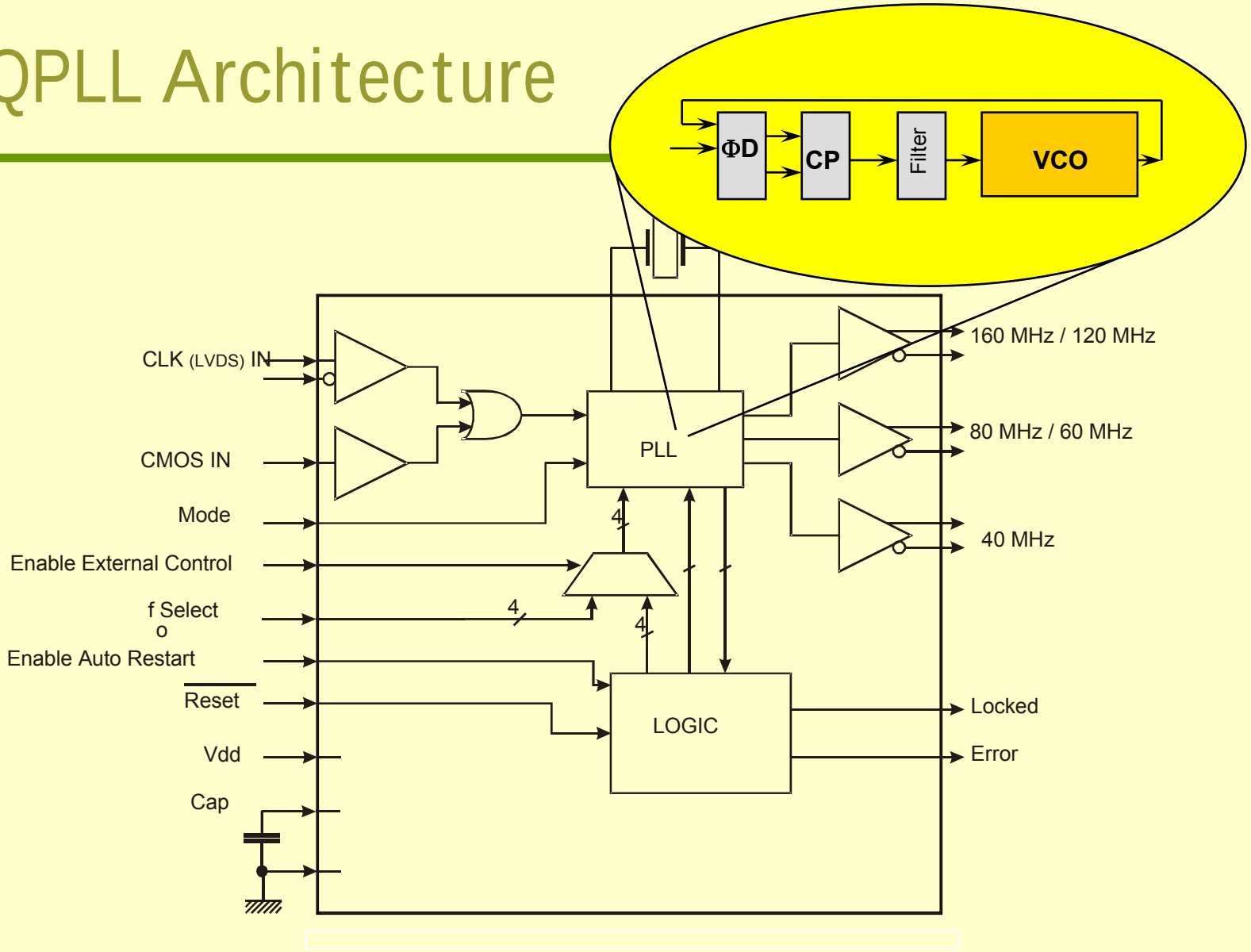
CERN-MIC

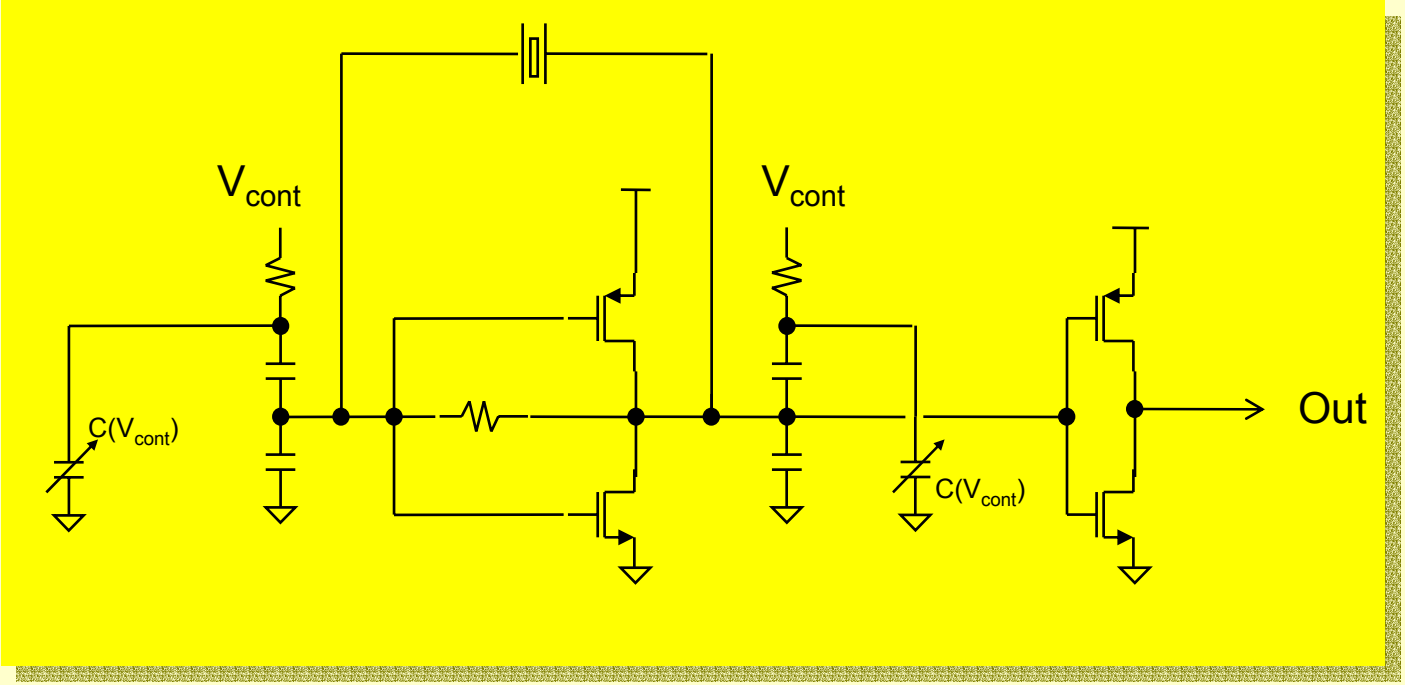
Outline

- QPLL Architecture and VCO Design
- Measured jitter
- Temperature and V_{dd} characterization
- Documentation
- Status and plans

QPLL Architecture



VCO (simplified) schematic



- Two contradictory requirements:
  - small jitter -> low VCO gain
  - cover entire process variation -> sufficiently high VCO gain

Nano course in VCO design

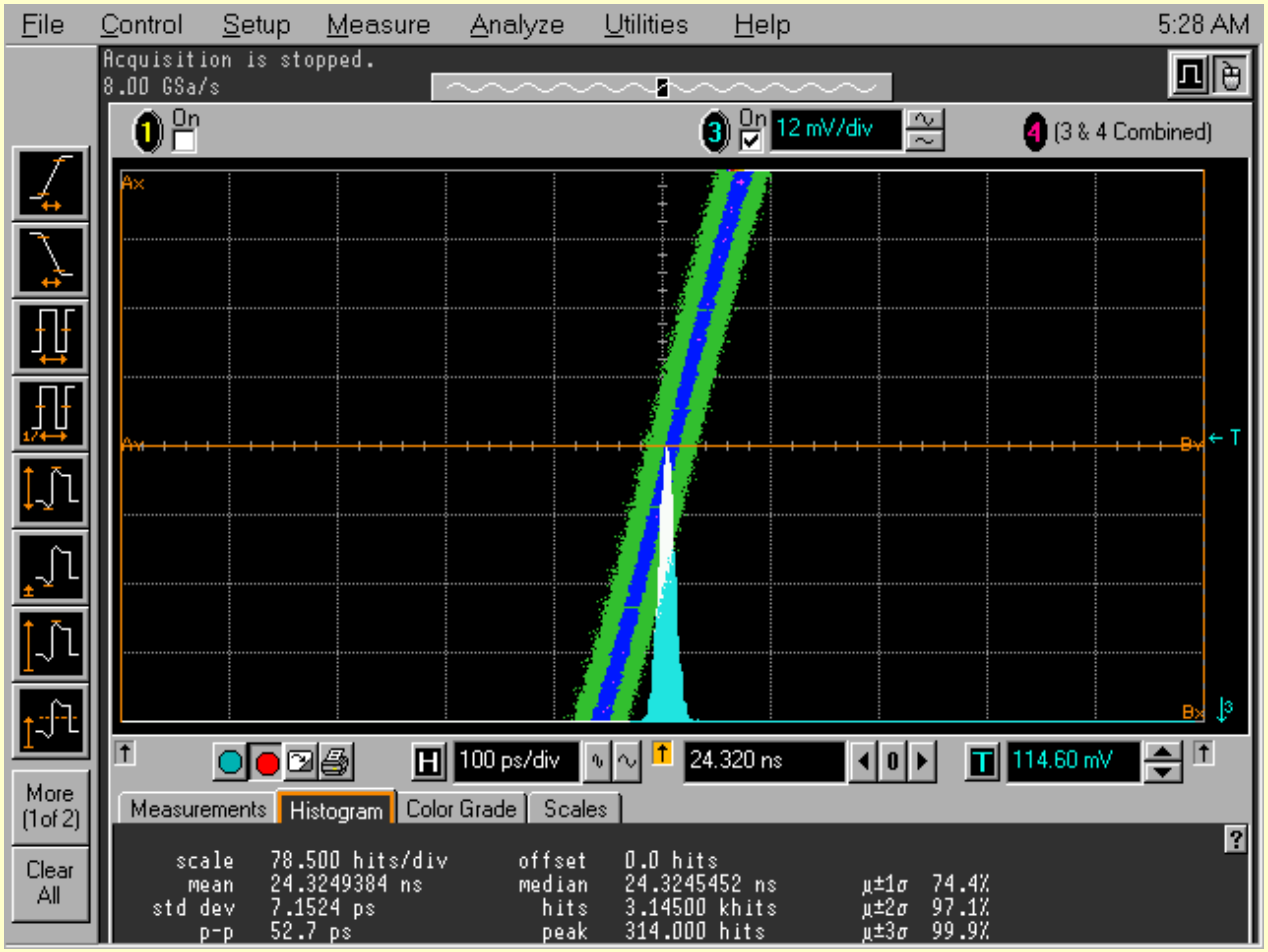
$$f = f(V_{cont})$$

- $f(V_{cont})$ smooth, such that any change in V_{cont} has a small influence on jitter

$$f = f(\text{process}, \text{Crystal}, \text{Temp}, V_{cont})$$

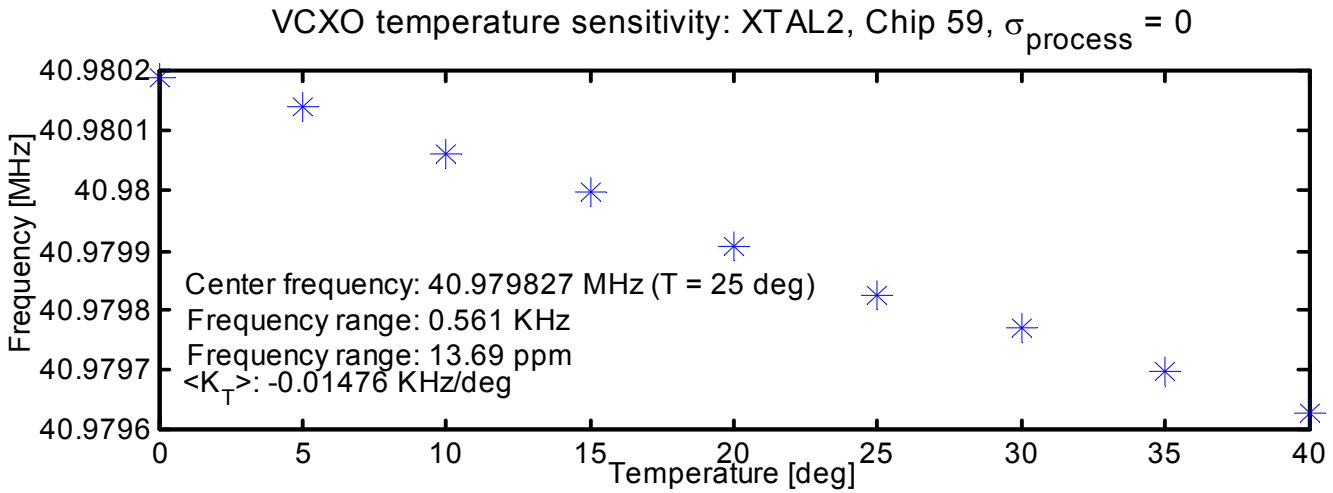
- $f_{min} < f(\text{process}, \text{Crystal}, \text{Temp}, V_{cont}) < f_{max}$

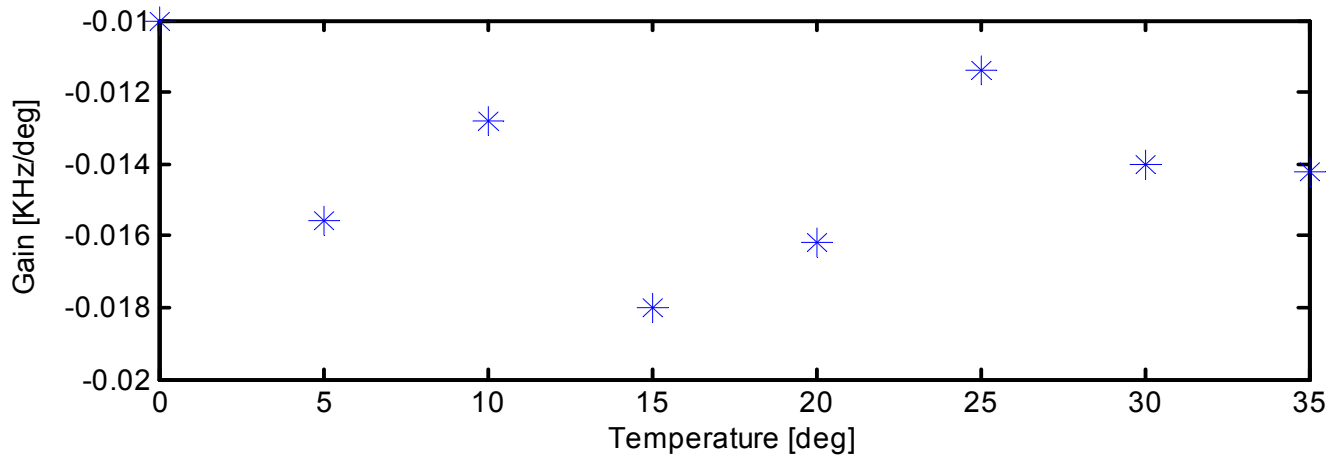
Jitter of VCO



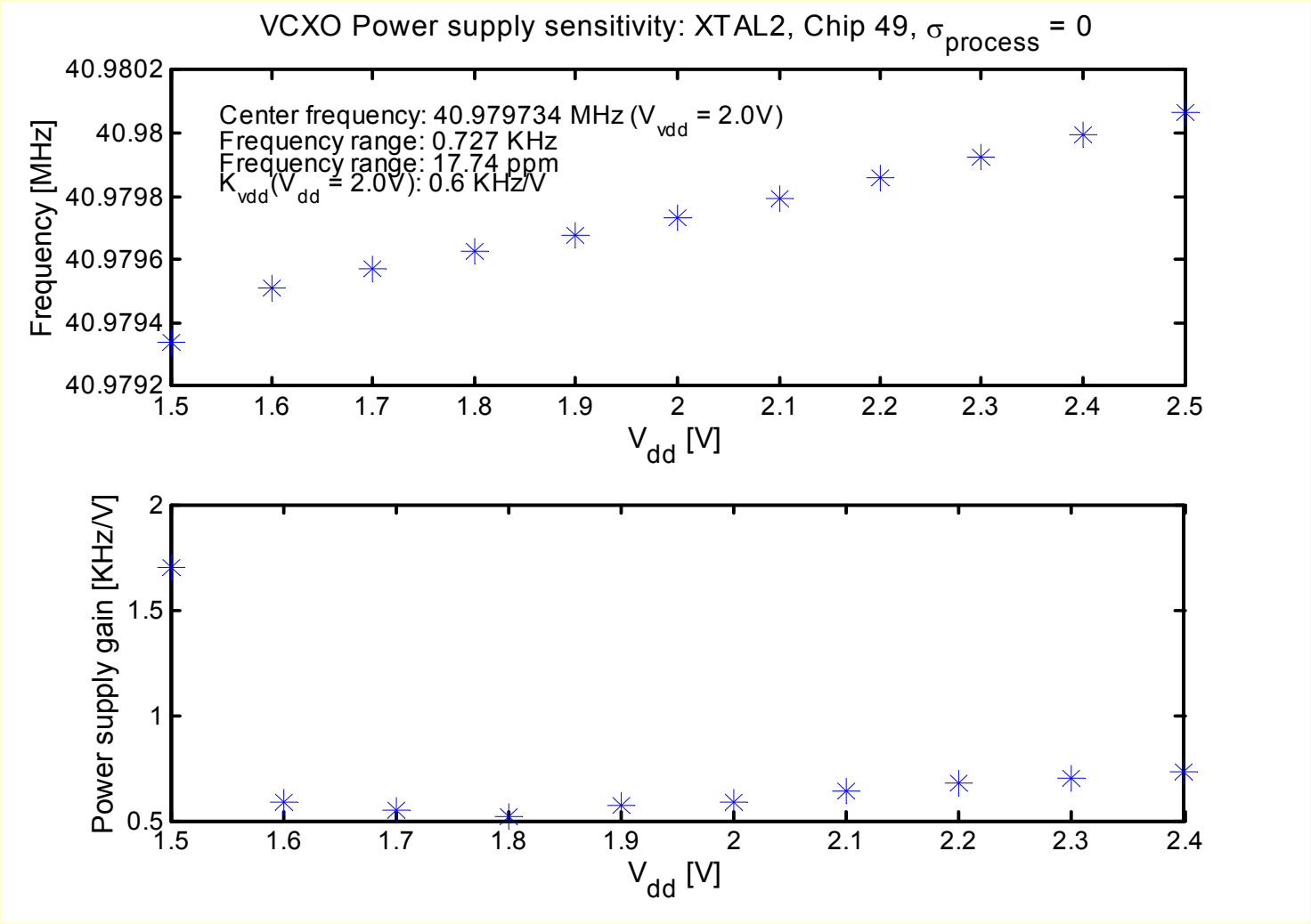
rms: 7.1 ps
p-p: 52.7 ps

Temp dependence

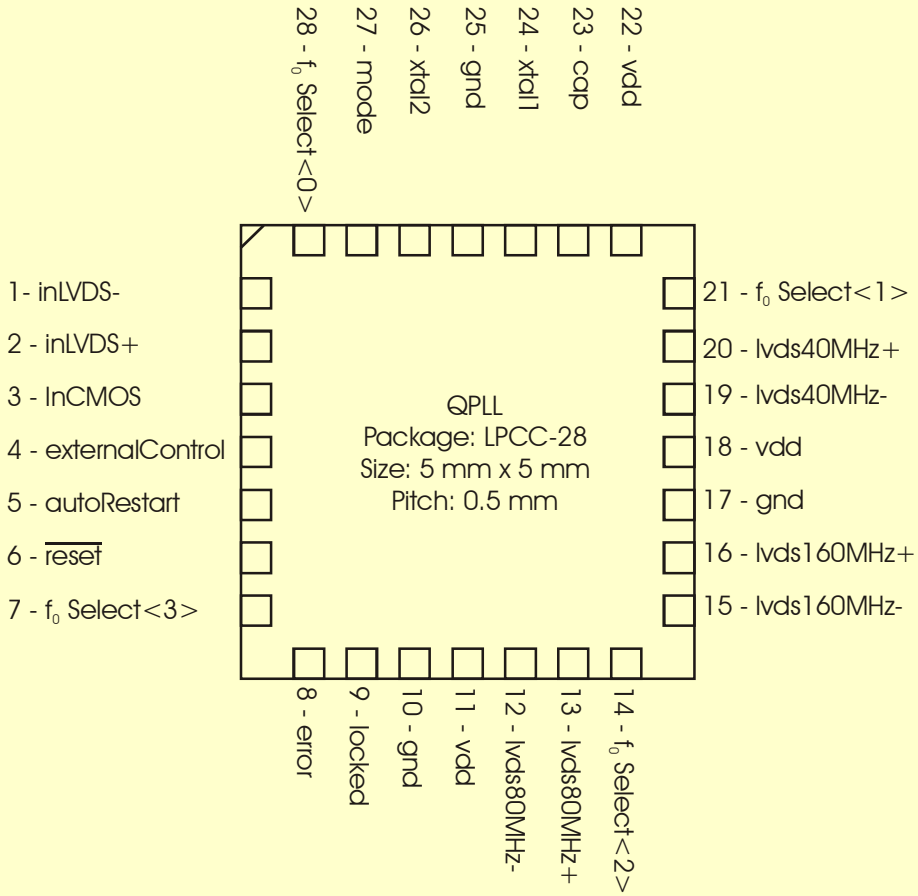




Vdd dependence



Final package proposal



Documentation

Preliminary data sheet

(including this talk) in:
http://proj-qpll.web.cern.ch/proj-qpll

Status and Plans

- Full QPLL submitted on an MPW in September
- Sample expected by mid December
- Package defined: LPCC28 pins, 5x5 mm
  - Must be packaged in final carrier
  - Order already issued
- Characterized by February with approx X-tal
- Custom *freq* X-tal ordered in March
- Samples in April
- Need "recommended" board layout
  - will be available from MIC to users

Answers to some FAQ

- Production order is being organized, but:
  - Must share production with other project !
    - » Silicon price depends on how this is organized
  - Need final quantity number !
  - Need to specify temperature range ! (asap)*
- Packaging: 0.30 CHF (NRE already paid)
- Testing: 0.40 CHF (+ NRE: ~ 10,000 CHF)
- Crystals:
  - ~12 CHF/pc (-10 to 60 deg C) t.b.c.

* = As small as possible