QPLL Status – May 2003

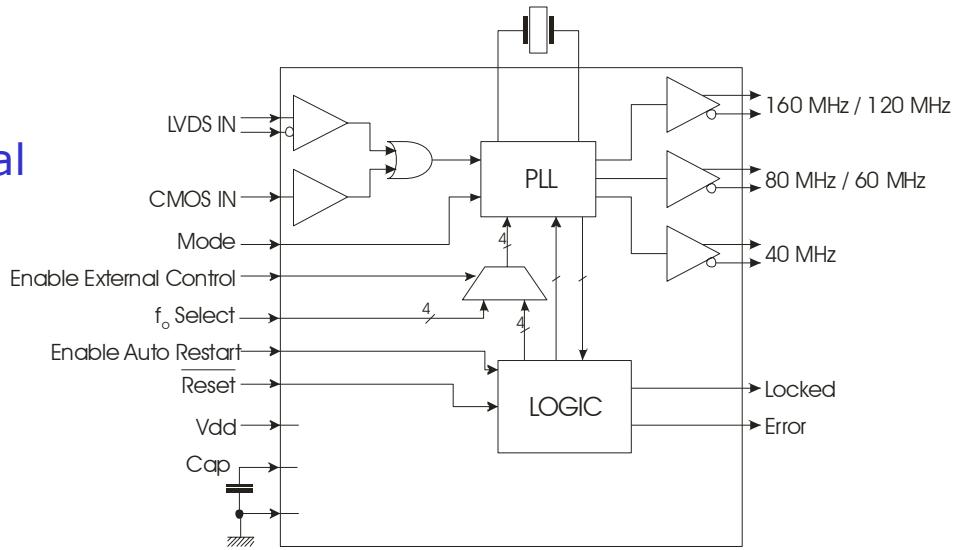
Paulo Moreira

Outline

- What's the QPLL?
- QPLL evaluation tests
- Data transmission tests
- June MPW
- Crystals
- TTCrq

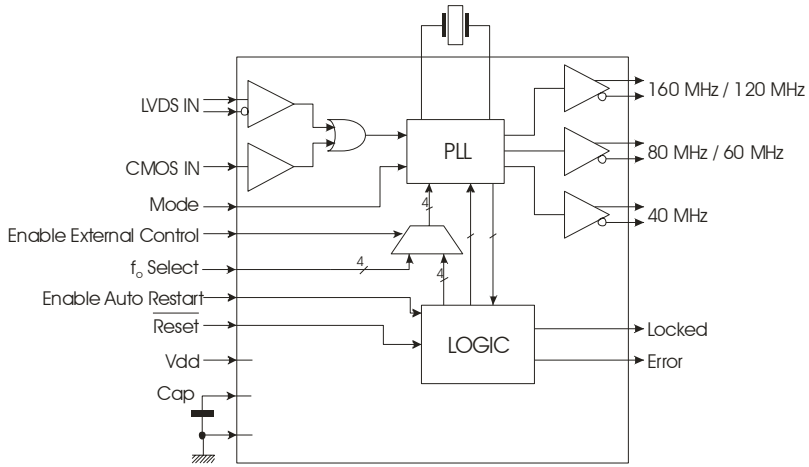
What's the QPLL?

- The QPLL is a Phase-Locked Loop made with a Voltage Controlled Crystal Oscillator (VCXO).
- Advantages:
  - Spectral purity of crystal oscillators
  - Phase and Frequency tracking ability of a PLL
- Disadvantages:
  - Narrow lock range
  - Custom tailored Quartz Crystal required
- Main purpose:
  - To act as a jitter filter for the TTC system



What's the QPLL?

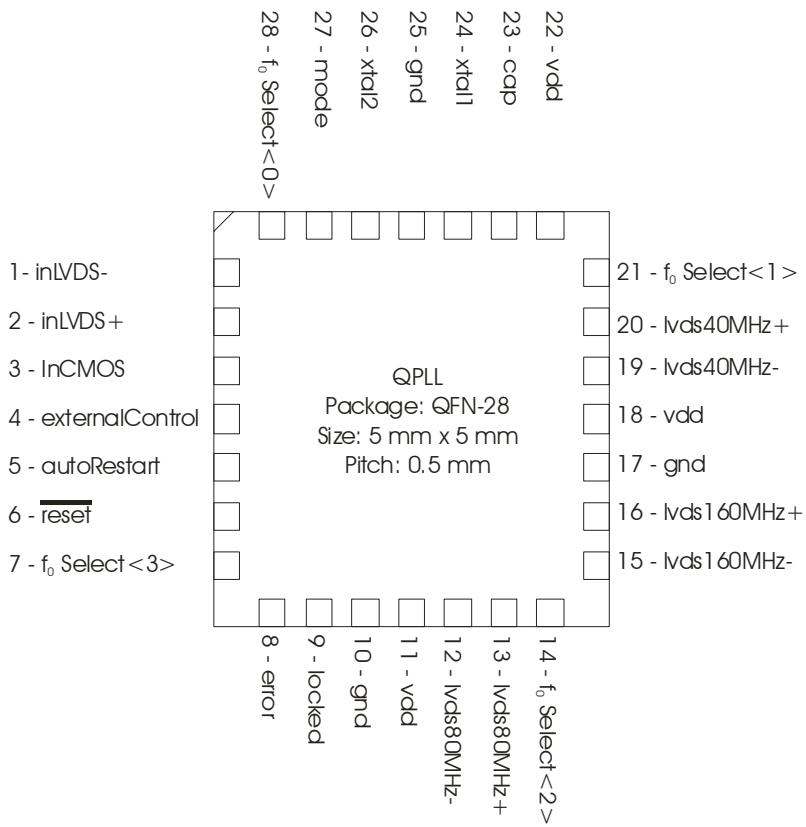
- Generates three clock signals, frequency and phase locked to the LHC master clock:
  - Mode 1:
    - 160 MHz
    - 80 MHz
    - 40 MHz
  - Mode 2
    - 120 MHz
    - 60 MHz
    - 40 MHz
  - The two clock multiplication modes require differently cut crystals.
- All the output clock signals are LVDS levels



- The reference clock input can be either:
  - LVDS
  - CMOS (5 V compatible)
- All the other inputs are CMOS 5 V compatible.
- Locked and Error flags are 2.5 V CMOS

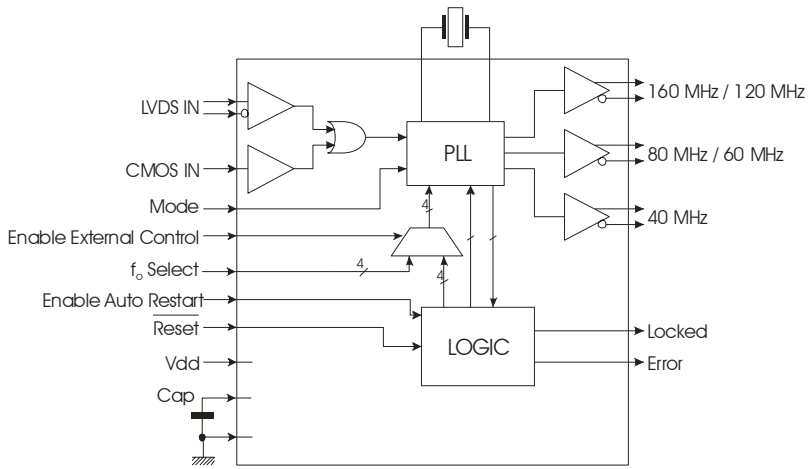
What's the QPLL?

- Package:
  - Plastic
  - QFN-28
  - 28 pins
  - 5 mm × 5 mm
  - 0.5 mm pitch
- Package by:
  - Atlantic Technology
    http://www.atlantic1.co.uk/at1/index.htm



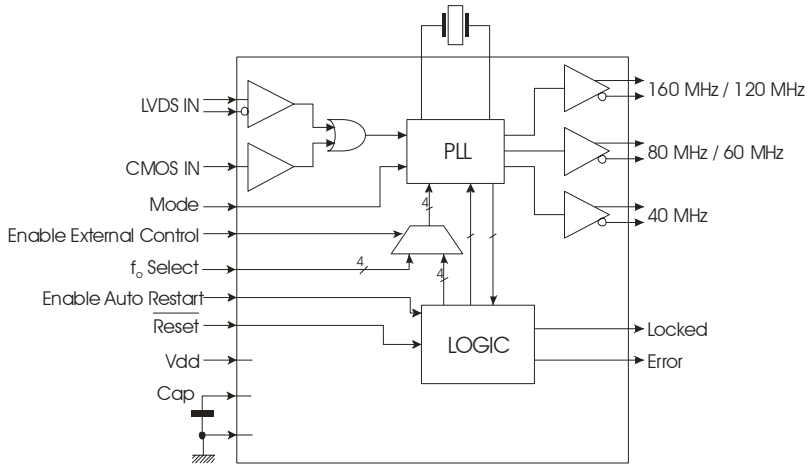
What's the QPLL?

- The narrow tuning range of a VCXO imposes several practical restrictions:
  - A custom crystal must be used
  - The crystal cut is made for a specific loading capacitance
  - Circuit parasitics due to PCB layout have an influence on the nominal frequency and tuning range.
  - CMOS "capacitors" have a limited capacitance versus voltage range (~3:1), further restricting the VCXO tuning range



What's the QPLL?

- The lock acquisition is done in two steps:
  - Frequency centering:
    - Capacitors are switched on/off until the VCXO free running frequency is as close as possible to the reference signal frequency (binary search)
  - Frequency and phase lock:
    - Once the VCXO frequency is chosen, the lock acquisition is done by the PLL control loop. The PLL will then lock by normal PLL action.
  - This process is automatic – no user action is required



- For testing purposes the locking procedure can be under the user control
- The QPLL automatically retries to lock if unlocked
- The automatic lock procedure can be disabled

QPLL evaluation tests

- Micro crystal kindly provided five crystals cut to 160.314744 MHz
- 20 QPLLs tested (all functional)

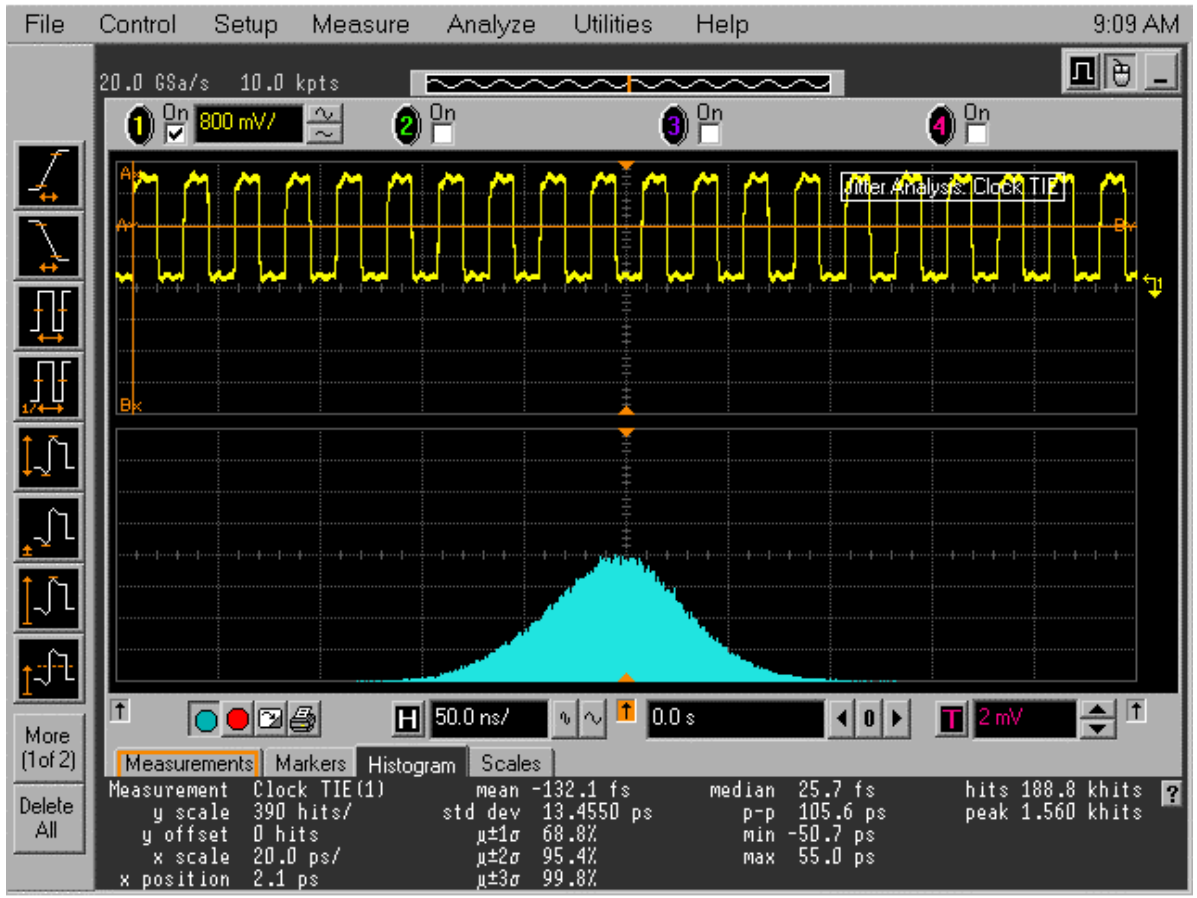
Crystal	f_{center} [MHz]	f_{offset} [kHz]	$C_{circuit}$ [pF]	Digital Range [kHz]	<Analog Range> [kHz]	f_{lock} (min) [MHz]	f_{lock} (max) [MHz]	Lock Range [kHz]
1	40.076958	-1.728 (-43 ppm)	4.45	3.422 (85 ppm)	2.873 (72 ppm)	40.074163	40.080523	6.360 (159 ppm)
2	40.077590	-1.095 (-27 ppm)	4.40	3.244 (81)	2.717 (68)	40.074933	40.080973	6.040 (150 ppm)
3	40.077060	-1.626 (-41 ppm)	4.48	3.119 (78 ppm)	2.627 (66 ppm)	40.074534	40.080344	5.810 (145 ppm)
4	40.076946	-1.740 (-43 ppm)	4.49	2.985 (74 ppm)	2.488 (62 ppm)	40.074516	40.080087	5.571 (139 pp)
5	40.076633	-2.053 (-51 ppm)	4.55	2.944 (74 ppm)	2.464 (62 ppm)	40.074237	40.079727	5.490 (137 ppm)

QPLL evaluation tests

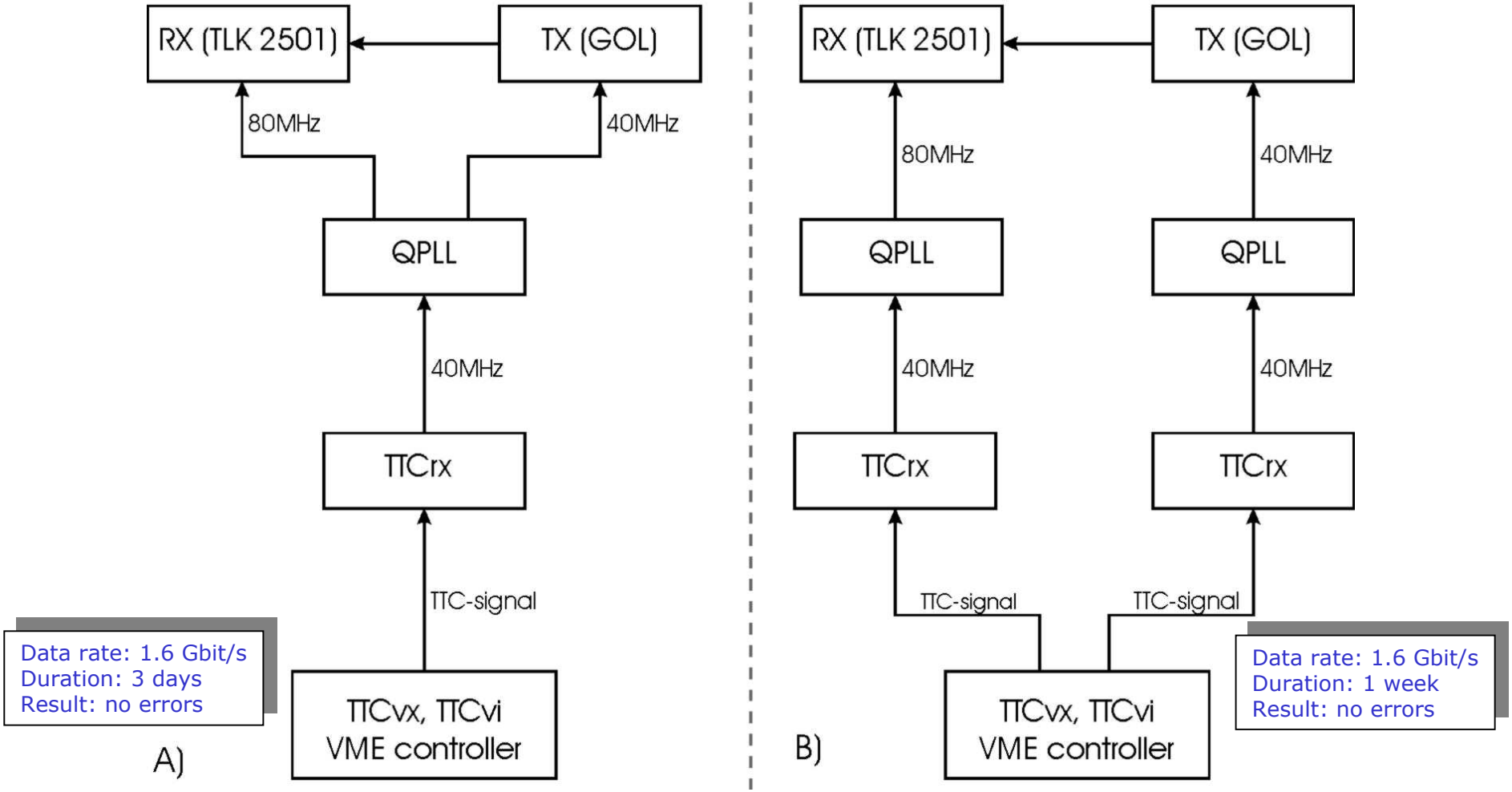
Jitter measurement:
Chain: TTCvi + TTCvx + TTCrx + QPLL
(Data + Triggers)

Cycle-to-cycle jitter:

RMS: 13 ps
P-P: 106 ps



Data transmission tests



June MPW

- The QPLL will be included in the MPW11 (23rd June)
- A few modifications:
  - Extend the digital tuning range
  - Reduce the power supply sensitivity
  - Improve jitter performance
- All modifications consider low risk. However, to avoid bad surprises, the "old" design will be resubmitted

Crystals

- The QPLL requires a custom cut Quartz Crystal for correct operation.
- Market survey for Quartz Crystal suppliers:
  - 10K to 15K parts required
  - Seven Crystal manufactures consulted
  - Micro Crystal (Switzerland) selected
    - Lead time: 14 weeks
- Users anxious for parts…!
- … but so far no budget code(s)!?

TTCrq

- A TTCrx + QPLL mezzanine card was developed
  - Can be mounted on a standard VME unit
  - Preserves the TTCrm functionality
  - Adds the QPLL functionality
  - J1 and J2 connectors pinout maintained
  - J3 connector added (QPLL)
  - The QPLL can be driven either from the TTCrx or from an external source
- User support from the CERN's electronics pool under discussion