Quartz Crystal Phase-Locked Loop (QPLL)

Features:

· Quartz crystal based PLL

Operation frequency: f(LHC) = 40.0786 MHz

Two frequency multiplication modes:

• ×4. ×2 and ×1

• ×3, ×1.5 and ×1

Locking range: ∆ ≈ ±4 KHz

Description:

The QPLL is a Quartz crystal based Phase-Locked Loop. Its function is to act as a jitter-filter for clock signals operating at the LHC clock frequency.

Depending on the operation mode, it provides three LVDS clock outputs at frequencies 160 MHz. 80 MHz and 40 MHz or 120 MHz, 60 MHz and 40MHz. The three outputs are synchronous with the input clock reference.

Pinout:

Loop bandwidth: < 7 KHz 28 - f₀ Select<0> 27 - mode 26 • Output jitter: < 50 ps peak-to-peak for input cap xtal gnd xtal Vd o signal jitter less than 120 ps RMS. Power supply voltage: 2.5V Power consumption: 100 mW 1- inLVDS-21 - f. Select<1> Reference clock inputs: 2 - inLVDS+ 20 - lvds40MHz+ LVDS 3 - InCMOS 19 - lvds40MHz-QPLL Package: Single-ended 5V compatible Size: 5 mm x 5 mm 18 - vdd 4 - externalControl Pitch: 0.5 mm Three LVDS clock outputs 17 - gnd 5 - autoRestart / f. Select<4> 16 - Nds160MHz+ 6 - reset 7 f. Select < 5> Package: LPCC-28 (5 mm x 5 mm, 0.5 mm pitch) 15 - lvds160MHz-7 · f. Select<3> Radiation tolerant 0.25 µm CMOS technology 10 12 3 - locked - erro - gnd vdd Nds80MHz Nds80MH Crystal: The QPLL will be provided together with Select<2: a Quartz crystal for operation at the specified frequency. Xtal2 Xtal1 160 MHz / 120 MHz LVDS IN PH 🕻 80 MHz / 60 MHz CMOS IN Mode 40 MHz **External Control** 0 f_Select<3:0> Auto Restart / f. Select<4> Reset / f. Select<5> ►Locked LOGIC Vdd ➤ Frror Voltage Cap regulator QPLL2/3

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