QPLL – a Quartz Crystal Based PLL for Jitter Filtering Applications in LHC

Paulo Moreira and Alessandro Marchioro

CERN-EP/MIC, Geneva Switzerland

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Outline

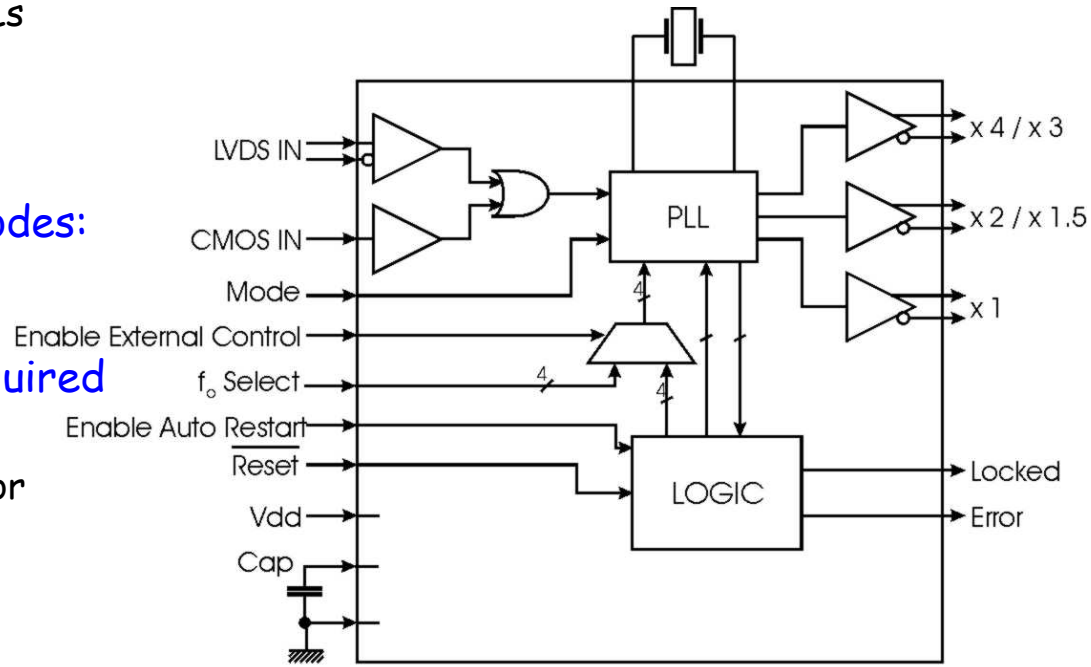
- Introduction
- QPLL overview
- QPLL operation
  - Circuit principles
  - Radiation tolerance
- QPLL Quartz Crystal
- Experimental results:
  - Jitter
  - Data transmission tests
- Future

Introduction

- LHC experiments use Gbit/s communication links
- Links run synchronous with the LHC master clock
- TTC is the system used to broadcast timing information
- TTCrx it the receiving end of the TTC system
- TTCrx jitter is not compatible with Gbit/s serializer requirements
- A VCXO based Phase Locked-Loop (the QPLL) was developed to overcome this problem
- The QPLL can be used as Jitter filter in the TTC system
- The QPLL can act as a clock reference for:
  - Gbit/s Serializers and Deserializers
  - Time-to-Digital Converters
  - Analogue-to-Digital Converters

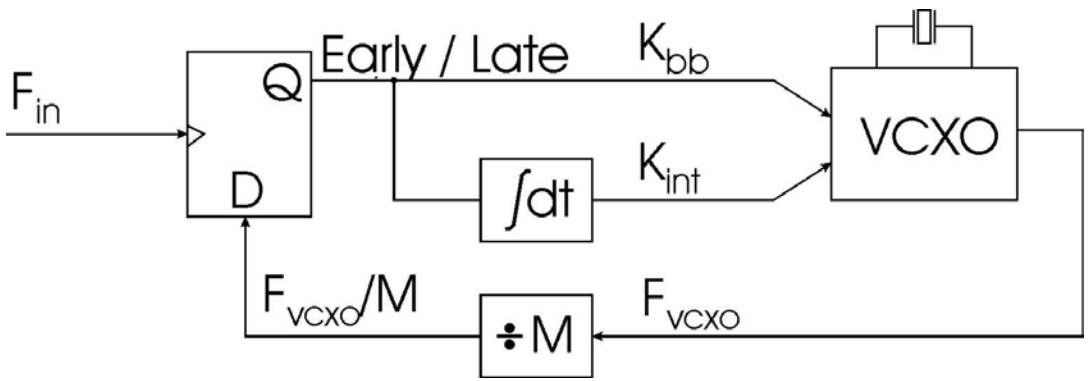
QPLL Overview

- QPLL: a PLL based on a VCXO:
  - VCXO – intrinsic low phase noise
  - Ideal for narrow band PLLs
  - Ideal for jitter filtering
- LHC nominal frequency:
  - 40.078666 MHz ±12 ppm
- Two clock multiplication modes:
  - ×1, ×2 and ×4
  - ×1, ×1.5 and ×3
- Custom Quartz Crystal required
- Stand alone operation:
  - Works as a clock generator
- Clock inputs:
  - CMOS, 5V tolerant
  - LVDS
- Other Inputs:
  - CMOS, 5V tolerant
- Package:
  - 28-pin LPCC (5 mm x 5 mm)



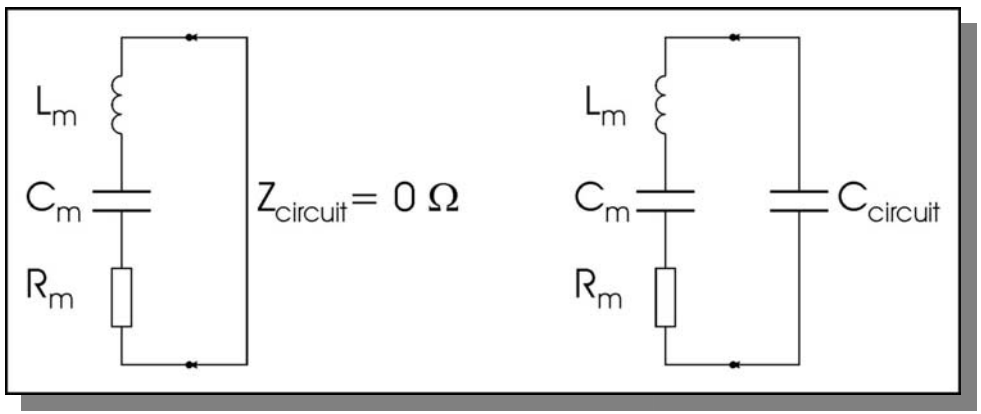
QPLL Operation

- Phase detector:
  - Bang-bang type
  - Only early/late decision
- VCXO
  - Two control ports
  - Bang-bang control
  - Continuous control
- Control loop:
  - Two control branches
  - Bang-bang: phase and frequency control
  - Integral: average frequency control
  - Almost independent optimization of K_{bb} and K_{int}



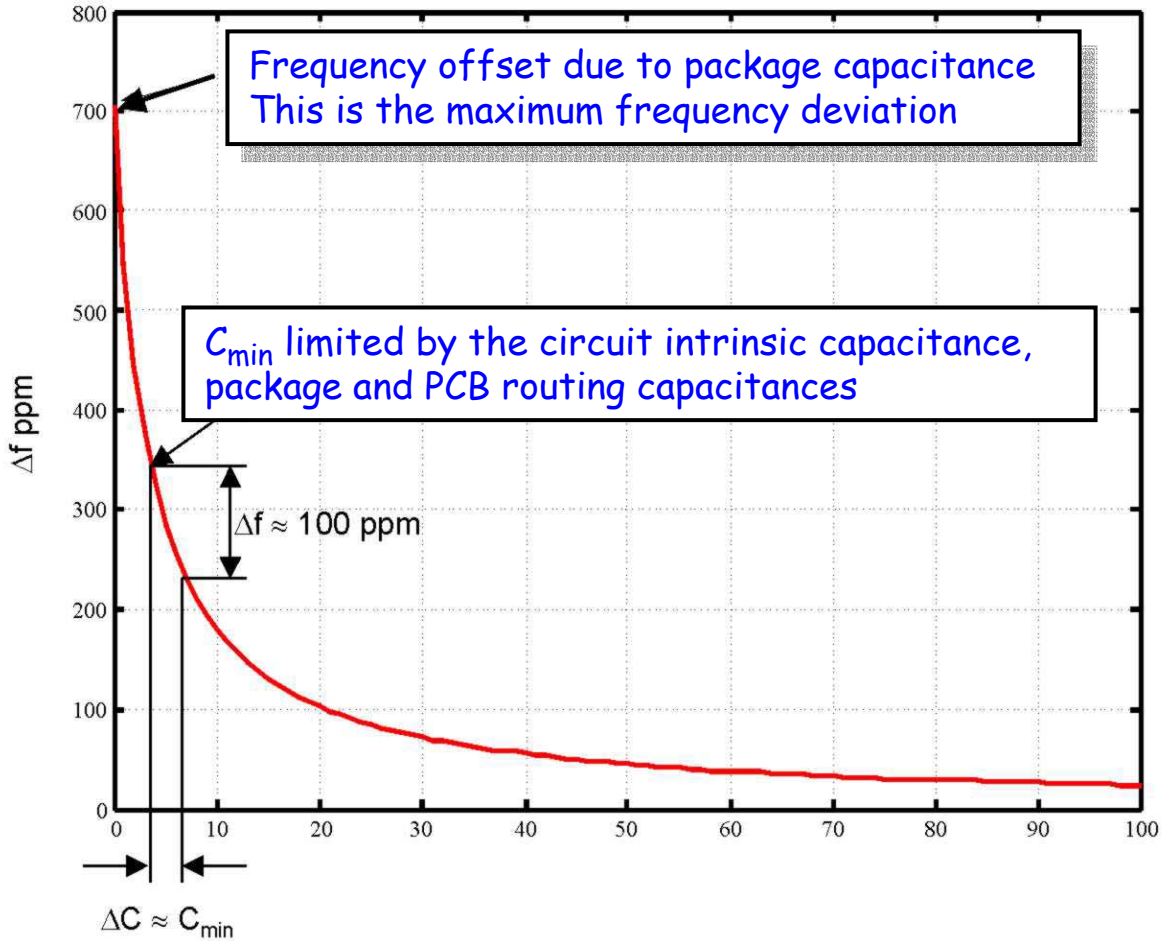
QPLL Operation

- Ideally the crystal should be loaded by a "short circuit":
  - The oscillation frequency will be the resonance frequency of the crystal: f_m
- In practice the oscillator presents a loading capacitance $C_{circuit}$ to the crystal:
  - The oscillation frequency is then higher than f_m;
  - Crystal manufacturing takes into account the loading capacitance
- The oscillation frequency can be controlled by changing the loading capacitance:
- The amount of control is very reduced:
  - C_m is orders of magnitude smaller than $C_{circuit}$
  - C_m : 5.9 fF
  - $C_{circuit}$: 3.4 pF to 5.5 pF
- Good: intrinsically low bandwidth PLL
- Bad: small locking range



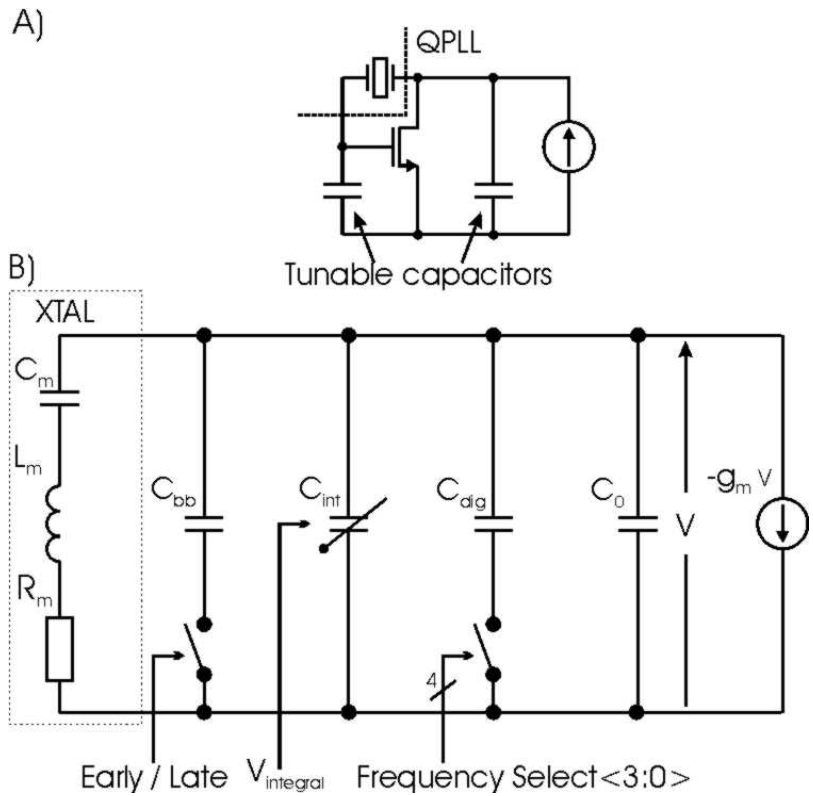
$$f_O = f_m \sqrt{1 + \frac{C_m}{C_{circuit}}}$$

QPLL Operation



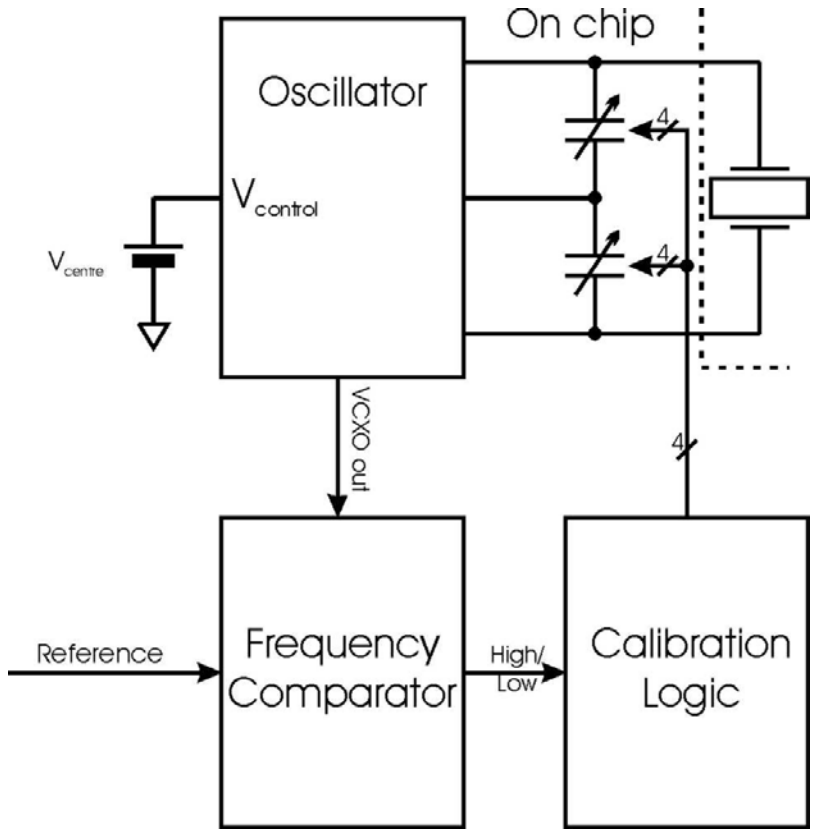
QPLL Operation

- VCXO:
  - Pierce Oscillator
  - Two frequency control capacitors
- Three frequency control mechanisms:
  - Bang-bang control:
    - switched capacitor
  - Integral control:
    - voltage controlled n-well capacitor
  - Frequency centering:
    - four binary weighted switched capacitors. (Not under the PLL loop control)



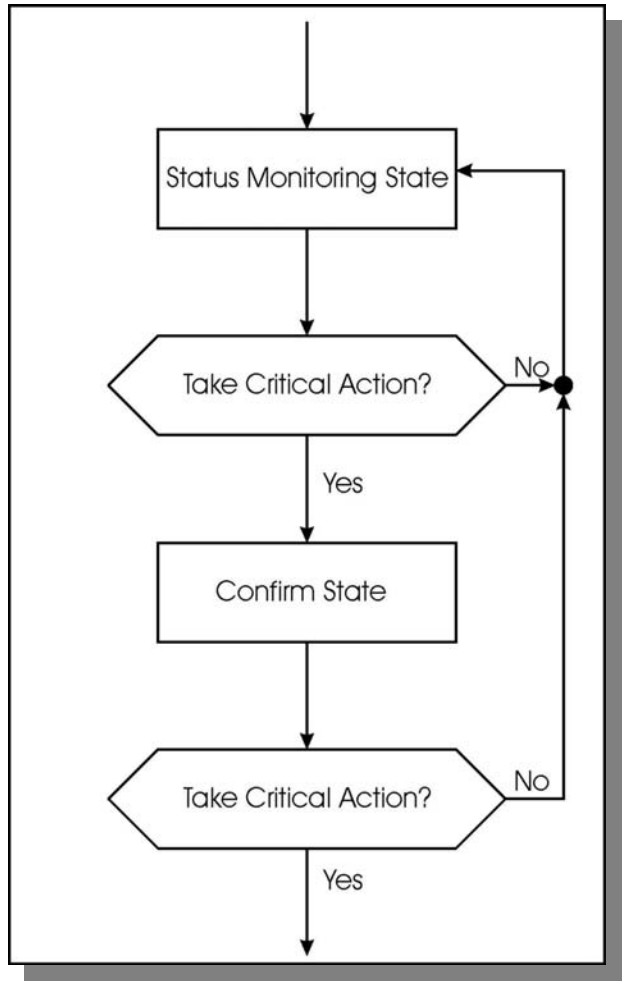
QPLL Operation

- Lock acquisition, two phases:
  - Frequency centering
  - Standard frequency pull-in and phase lock cycle
- Frequency centering:
  - After start-up, reset or unlocked operation detected
  - Frequency-only detector used
- Frequency centering operations:
  1. The bang-bang loop is disabled
  2. The VCXO control voltage forced to its mid range value
  3. A binary search is made to decide on the value of the frequency centering capacitor
  4. Once the value found, control is passed to the PLL control loop
- The frequency centering operation can be disabled:
  - In this case the user has to program the correct capacitor value
  - Useful to prevent unwanted calibration cycles
  - Or to use the QPLL as a simple crystal oscillator



Radiation Tolerance

- Total dose:
  - 0.25 μm CMOS process
  - Enclosed NMOS
  - Guard rings
- Single Event Upsets:
  - Majority voting circuits
  - Confirm before acting
  - When in doubt, take the action with less impact for the system



Quartz Crystal

- For operation on the x1, x2 and x 4 mode, CERN will provide a crystal with each QPLL
- A contract has been signed with Micro Crystal for the production of 10K parts
- A first series of 100 parts has already been delivered for prototype evaluation
- Frequency tolerance taking into account:
  - LHC frequency: ± 12 ppm
  - Crystal: ± 31 ppm
    - Frequency tolerance
    - Drift over temperature range
    - Aging
  - QPLL circuit contribution: ± 7 ppm
  - Total: ± 50 ppm
- QPLL locking range:
  - Full range: ± 72 ppm

- Inverted mesa AT-Cut
- Resonance mode:
  - Fundamental
- Load Frequency:
  - 160.314744 MHz
- Load Capacitance:
  - 4.48 pF (typical)
- Frequency Tolerance at 25°C:
  - -18 to 18 ppm
- Drift over Temperature Range:
  - -10 to 10 ppm
- Aging first year:
  - ± 3 ppm
- Motional Capacitance:
  - 4.2 fF (min)
- Static Capacitance:
  - 2.8 pF (typical)
- Drive Level:
  - 100 µW (max)
- Operating Temperature Range:
  - 0 to 60 °C
- Series Resistance at 25 °C:
  - 35 Ohm (maximum)
- Package type:
  - SMD ceramic CC1F-T1A
  - 8 mm x 3.7 mm x 1.75 mm

Jitter

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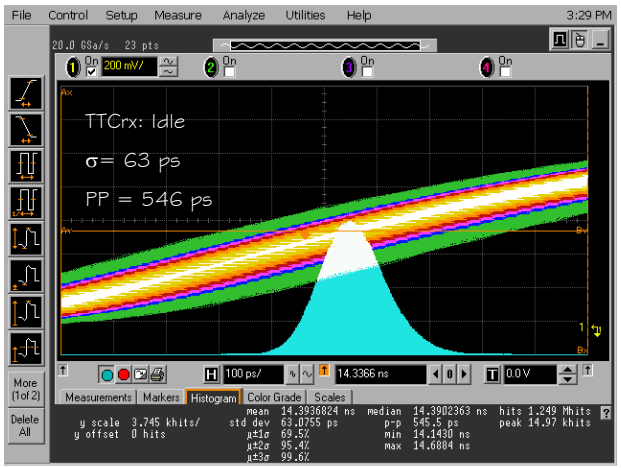

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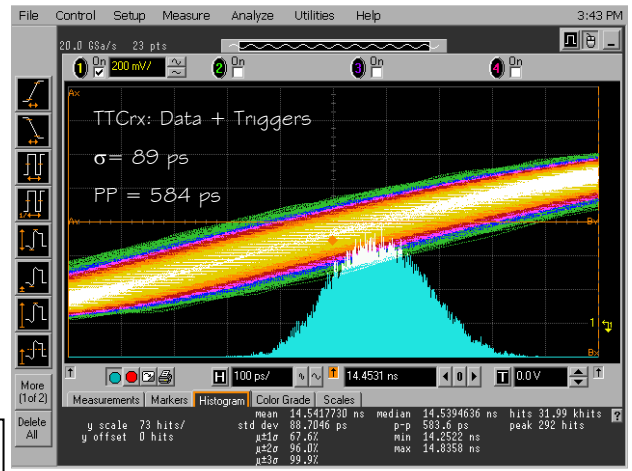

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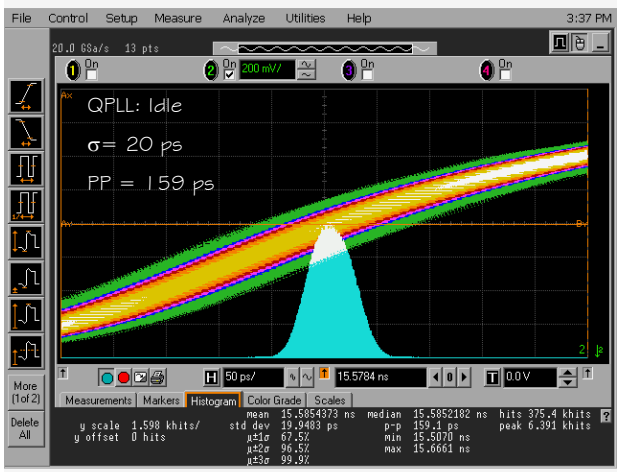

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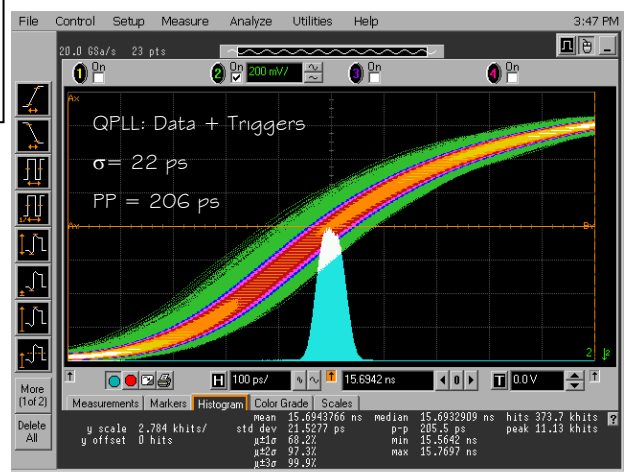
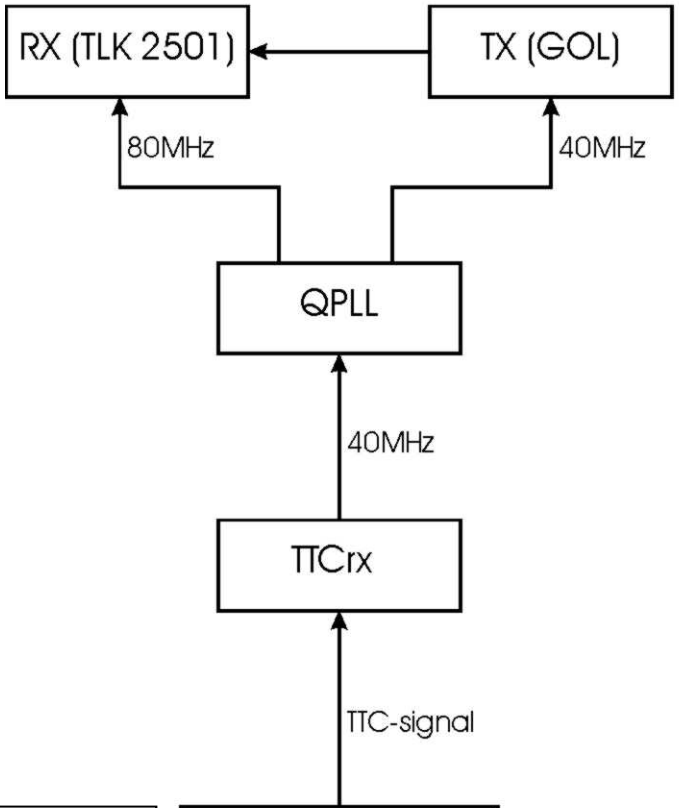


54855A Infinium Oscilloscope

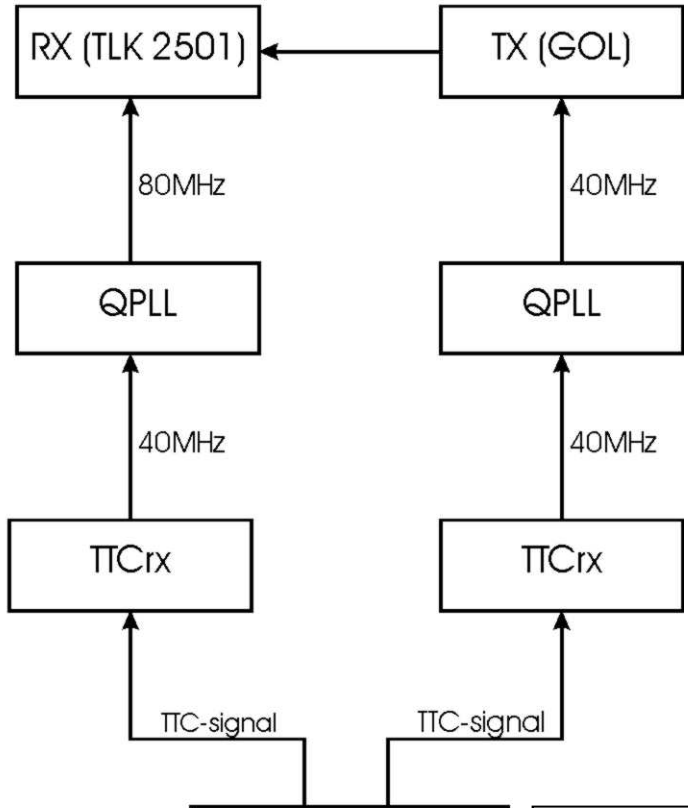
- Analog bandwidth: 6 GHz
- Real-time sampling
- Sample rate: 20 GSa/s

Data Transmission Tests



Duration: Three days

Result: Error free



Duration: One week

Result: Error free

Past and (Near) Future

- A second version of the QPLL was developed
  - Expanded lock range: +50 %
  - Includes internal supply regulator
  - The new chip is functionally and pinout compatible
  - Two of the pins have now double functionality:
    - If "internal control": Everything as before
    - If "external control":
      - nReset → frequencySelect<5>
      - autoRestart → frequencySelect<4>
- Schedule:
  - Design submitted for fabrication: July
  - Wafers received from the foundry: September
  - Wafers shipped for dicing: September
  - Chips shipped for packaging: September
  - Packaged chips received: Any time in October!
- The engineering run reticle contains:
  - 4 new QPLL – Total: 540 chips
  - 2 old QPLL - Total: 270 chips (safety measure)

Summary

- TTCrx clock jitter:
  - too high to serve as a clock reference for high speed data links
- A PLL based on a VXCO was developed to act as a Jitter filter in the TTC system
- The QPLL was produced in prototype quantities
  - The circuit is fully functional
  - Data transmission tests prove that it can be used as a clock reference for high speed serializers
  - Can also be used as a clock source for high resolution TDCs and ADCs
  - The QPLL can also be used "standalone" as a clock generator
- A new design with increased locking range will be tested soon
- October 2003 devices will be available:
  - QPLL1: 270 pieces
  - QPLL2: 540 pieces