Voltage Controlled Quartz Crystal Oscillator (VCXO) ASIC

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General:

The VCXO ASIC is a test structure designed by the CERN microelectronics group in a commercial 0.25 μm CMOS technology using radiation-tolerant layout techniques.
This design was a first step towards the development of a quartz based PLL for jitter filtering applications (see QPLL).
The block diagram of the VCXO IC is represented on Figure 1. The ASIC is composed of a voltage controlled quartz crystal oscillator and of a clock divider. The clock divider can be set to generate the following output frequencies:

- 40 MHz and 80 MHz for a 160 MHz fundamental frequency crystal;
- 40 MHz and 60 MHz for a 120 MHz fundamental frequency crystal.

There are two mechanisms for control of the oscillation frequency:

- By setting a binary number on the four digital control inputs (RS<3:0>);
- By setting a voltage level on the analogue frequency control input (V(contol)).

The digital control is used to set the frequency range while the analogue input allows changing the oscillation frequency in a continuous manner for a given frequency range.

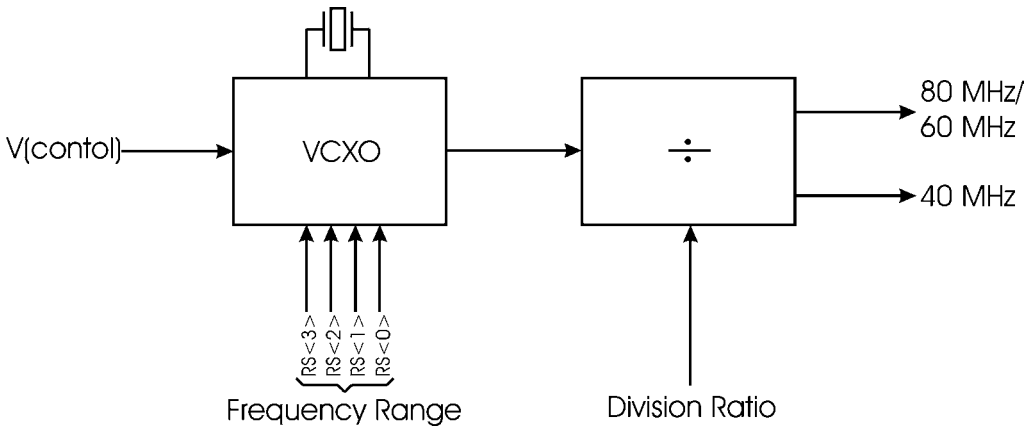


Figure 1 Voltage controlled crystal oscillator block diagram

The ASIC was tested in conjunction with an inverted mesa AT cut quartz crystal fabricated by Micro Crystal Switzerland. The mode of vibration for these crystals is the fundamental. The samples tested were cut to operate at the nominal frequency of 163.384 MHz with an "infinite" load capacitance. The crystal is packaged in a SMD ceramic package (CC1F-T1A).

Test setup

The test setup used for the frequency measurements is represented in . The VCXO circuit was tested under temperature-controlled conditions. A test card containing the VCXO was installed inside a temperature controlled "oven". Power to the ASIC was provided from the outside using the "+6V" output of the Agilent E3631A programmable power supply. The second output ("+25V") was used to generate the VCXO control voltage.
A group of five switches was used to set the VCXO frequency. One of them controls the division ratio of the clock divider while the other four control the oscillator frequency range. The value set by these switches was changed during the tests. To avoid having to wait for the "oven" temperature to stabilize each time they were changed, these switches were external to the "oven".
The 40MHz clock output was connected to the HP 8447A amplifier using a 50Ω coaxial cable. The amplifier was then connected to the SRS SR620 frequency meter that was used to measure the signal frequency.

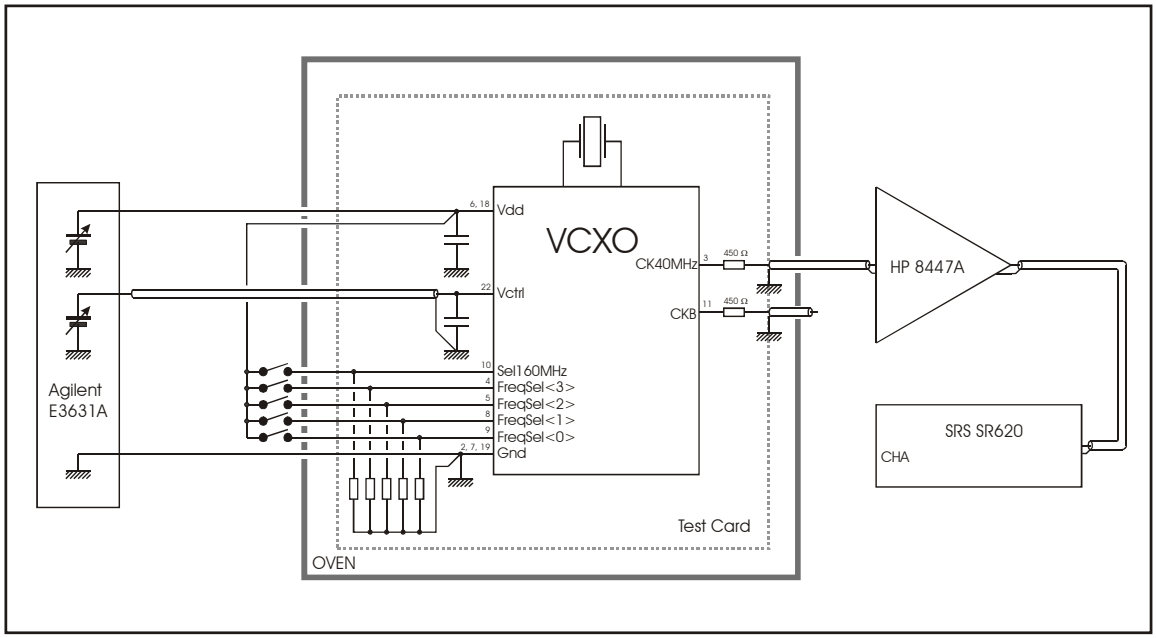


Figure 2 VCXO test setup

During the tests, it was found that the small thermal inertia of the ASIC/XTAL was posing problems to the measurement stability. With the exception of the temperature sweep tests, it was considered better to do the measurements under ambient temperature conditions - which was stable enough for its effect not to be noticeable on the measurements.

Crystals

Three crystals cut for the same nominal frequency were used during the tests. The crystals were successively bonded to several ASICs to estimate the variability introduced by the ASIC on the oscillation frequency and tuning range.
The series resonance frequency of each crystal is given in Table 1. The values of the resonance frequency are given for "infinite" load capacitance.

Crystal	Resonance frequency [MHz]	Motional capacitance [fF]	Shunt capacitance [pF]
1	163.835554	4.07	2.75
2	163.847643	5.94	2.74
3	163.845441	6.12	2.78

Table 1 Crystals resonant frequencies

ASICs

During ASIC production the wafers were "striped" to produce gate lengths going form $0.85 \times$ L(nominal) to $1.25 \times$ L(nominal) across the wafer. In this document, "$\sigma_{process}$" gives an indication of the transistors gate length:

$\sigma_{process} = -3 \rightarrow L = 0.85 \times L_{nominal}$,
$\sigma_{process} = 0 \rightarrow L = L_{nominal}$,
$\sigma_{process} = +3 \rightarrow L = 1.25 \times L_{nominal}$.

Stray capacitance

To estimate the impact of the package and PCB routing capacitance all the tests were repeated with two 3.3 pF capacitors connected between each on of the crystal terminals and ground. In the tables this case corresponds to: $\sigma_{process}$ & 3.3 pF

Test 1: Digital control transfer function

During this test, the temperature was maintained constant (≈20ºC), the power supply voltage was set to the nominal value (2.5V), the analogue control voltage set to 0.8V (approximately mid range) and the frequency division ratio set to 160 MHz (Sel160MHz = 1). The digital control input was swept and the output frequency (oscillation frequency/4) measured.
The results are summarized in Table 2. In this table, center frequency refers to the value measured for RS<3:0> = 1000 (binary), which corresponds to midrange, and the frequency step is the average value.

Crystal Number	Chip Number	$\sigma_{process}$	Center Frequency [MHz]	Frequency Range [KHz]	Frequency Range [ppm]	Frequency Step [KHz] (average)
1	27	-3 & 3.3 pF	40.971012	2.364	58	-0.158
1	27	-3	40.973000	3.409	83	-0.228
1	48	0	40.972740	3.273	80	-0.218
1	58	0	40.972681	3.163	77	-0.211
1	43	+3	40.972483	3.076	75	-0.205
2	46	-3 & 3.3 pF	40.976824	2.587	63	-0.172
2	46	-3	40.980072	4.217	103	-0.281
2	49	0	40.980070	4.242	104	-0.283
2	59	0	40.979794	4.098	100	-0.273
2	63	+3	40.979615	3.873	94	-0.258
2	83	-3 & 3.3 pF	40.976781	2.490	61	-0.166
3	83	-3	40.980063	4.176	102	-0.278
3	50	0	40.980138	4.334	106	-0.289
3	60	0	40.979792	4.362	106	-0.291
3	82	+3	40.979621	4.097	100	-0.273

Table 2 Digital control measurement results

For the same quartz crystal, the impact of the circuit on the central frequency is summarized in Table 3. Table 2 shows that there is a frequency trend with process ($\sigma_{process}$) – longer gate lengths corresponding to lower frequencies. In all cases, the circuit contributes less than 13 ppm (p-p) to the dispersion of the frequency values. As expected, similar values and behavior are found for the following three sets of measurements.

Crystal Number	Mean Frequency [MHz]	Standard Deviation [ppm]	Frequency Range [ppm]
1	40.972726	5.2	13
2	40.979888	5.5	11
3	40.979903	5.9	13

Table 3 Digital control measurement results: impact of the circuit on the center frequency

Typical curves of the digital transfer function are represented in Figure 3 for crystal 1 with four different ASICs. Figure 4 represents, for the same crystal and ASICs, the frequency step as function of the digital control number.

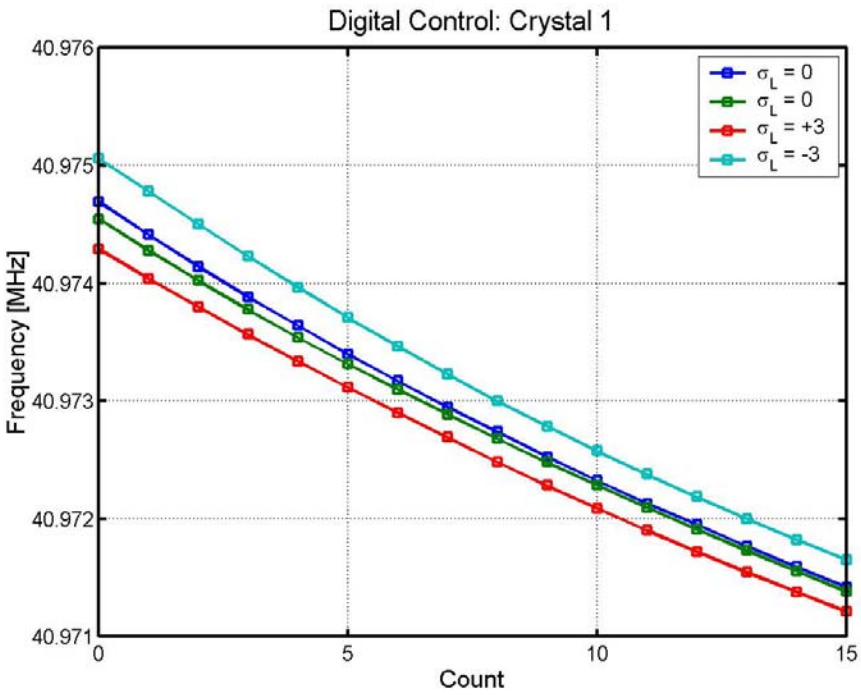


Figure 3 Digital transfer function (crystal 1 with chips: 27, 48, 58 and 43)

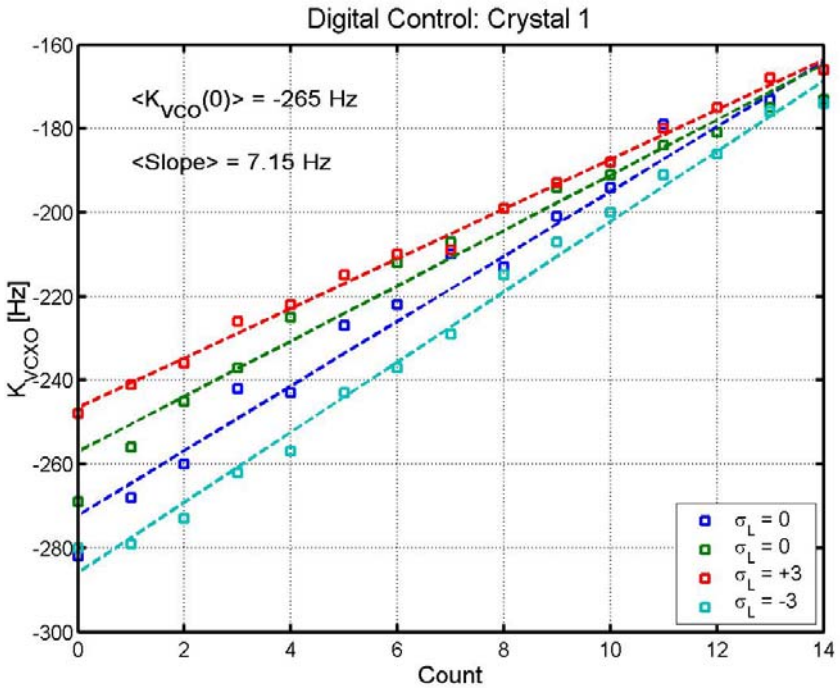


Figure 4 Digital transfer function: frequency step size as function of the digital control number (crystal 1 with chips: 27, 48, 58 and 43)

Test 2: Analogue transfer function

The analogue transfer function was measured under similar conditions. However in this case the digital control inputs were fixed to RS<3:0> = 1000 (binary) and the analogue voltage swept between 0 and 1.6 V. The measurement results are summarized in Table 4

Crystal Number	Chip Number	$\sigma_{process}$	Center Frequency [MHz]	Frequency Range [KHz]	Frequency Range [ppm]	K_{VCO} [KHz/V]
1	27	-3 & 3.3 pF	40.971011	1.335	33	-1.217
1	27	-3	40.972999	1.963	48	-1.740
1	48	0	40.972740	1.886	46	-1.660
1	58	0	40.972683	1.756	43	-1.623
1	43	+3	40.972485	1.819	44	-1.627
2	46	-3 & 3.3 pF	40.976824	1.356	33	-1.208
2	46	-3	40.980069	2.288	56	-1.980
2	49	0	40.980066	2.350	57	-1.960
2	59	0	40.979797	2.220	54	-1.917
2	63	+3	40.979615	2.196	54	-1.910
3	83	-3 & 3.3 pF	40.980061	2.234	54	-1.775
3	83	-3	40.980061	2.234	54	-1.775
3	50	0	40.980141	2.330	57	-1.845
3	60	0	40.979793	2.291	56	-1.983
3	82	+3	40.979615	2.146	52	-1.872

Table 4 Analogue control measurement results

Typical curves for the analogue transfer function are represented in Figure 5.

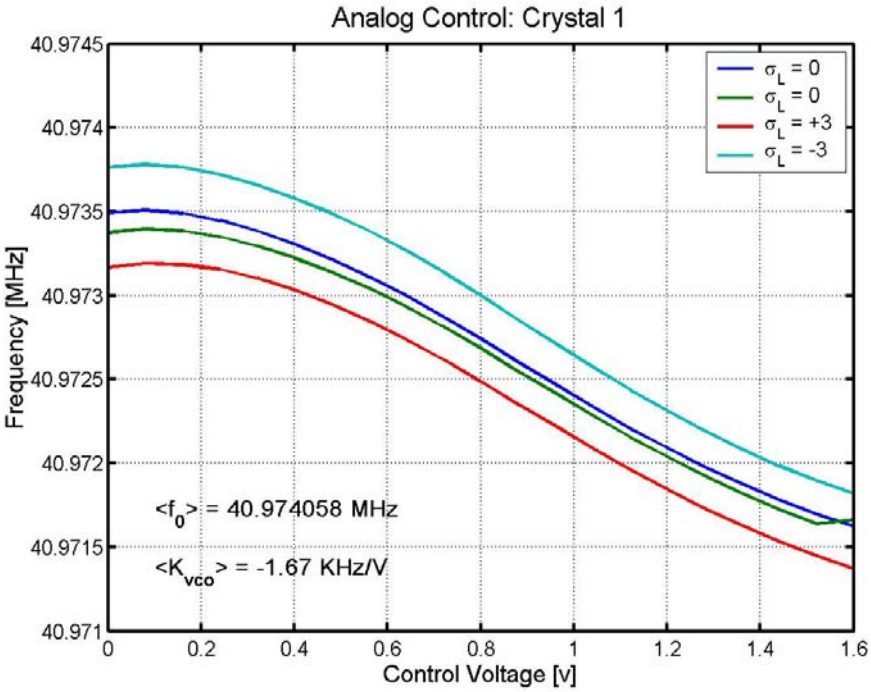


Figure 5 Analogue transfer function (crystal 1 with chips: 27, 48, 58 and 43)

Test 3: Power supply sensitivity

In this test both the digital control and the analogue control voltage were maintained fixed at their midrange values (V(control = 0.8V) and RS<3:0> = 1000 (binary)). The temperature was constant and the power supply voltage was swept from 1.5V to 2.5V.
The measurement results are summarized in Table 5. In this table, frequency and K_{VDD} are given for 2.0V power supply.

Crystal Number	Chip Number	$\sigma_{process}$	Frequency [MHz]	P-P Frequency [KHz]	P-P Frequency [ppm]	K_{VDD} [KHz/V]
1	27	-3 & 3.3 pF	40.970463	1.074	26	1.076
1	27	-3	40.972426	1.116	27	1.082
1	48	0	40.972147	1.164	28	1.130
1	58	0	40.972126	1.190	29	1.118
1	43	+3	40.971913	1.246	30	1.186
2	46	-3 & 3.3 pF	40.976405	0.765	19	0.772
2	46	-3	40.979809	0.486	12	0.434
2	49	0	40.979734	0.727	18	0.600
2	59	0	40.979556	0.522	13	0.426
2	63	+3	40.979355	0.772	19	0.622
3	83	-3 & 3.3 pF	40.976415	0.894	22	1.020
3	83	-3	40.979792	0.540	13	0.532
3	50	0	40.979785	0.665	16	0.682
3	60	0	40.979591	0.511	12	0.396
3	82	+3	40.979399	0.666	16	0.550

Table 5 Power supply sensitivity measurement results

Typical supply sensitivity curves are represented in Figure 6.

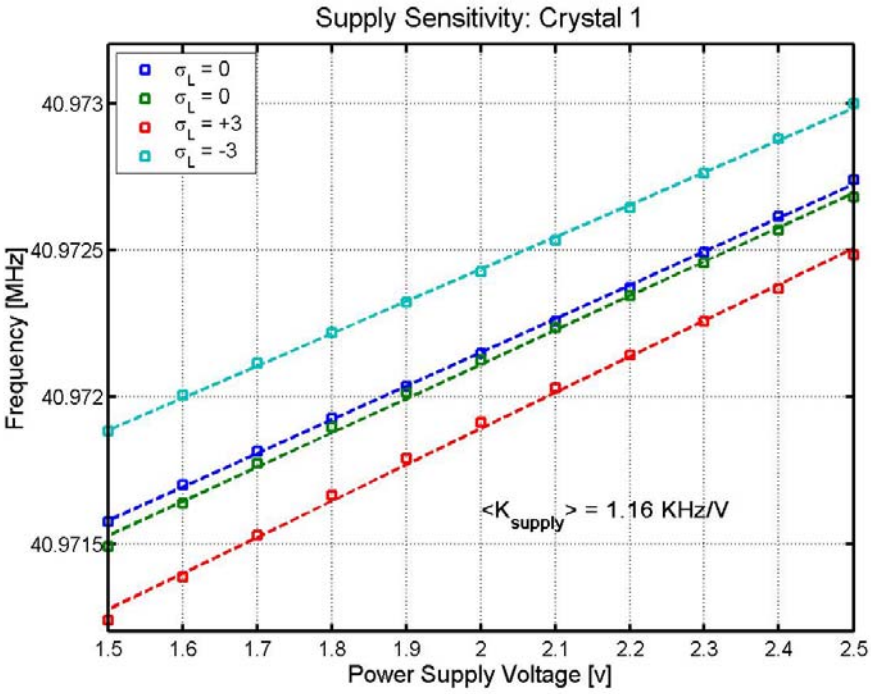


Figure 6 Power supply sensitivity (crystal 1 with chips: 27, 48, 58 and 43)

Test 4: Temperature sensitivity

During this test both the digital control and the analogue control voltage were maintained fixed at their midrange values (V(control = 0.8V) and RS<3:0> = 1000 (binary)). The power supply voltage was set to 2.5V and the temperature swept from 0 to 40°C. A temperature probe was placed in close proximity with the chip/crystal and the temperature control mechanism stopped during the measurement period – during which, the temperature indicated by the probe did not changed more than 0.1°C.

The measurement results are summarized in Table 6. In this table frequency and K_T are given for T=25°C

Crystal Number	Chip Number	$\sigma_{process}$	Frequency [MHz]	P-P Frequency [KHz]	P-P Frequency [ppm] For: $0 \le T \le 40$ °C	K_T [KHz/°C]
1	27	-3 & 3.3 pF	40.970732	0.682	17	-0.017
1	27	-3	40.972998	0.754	18	-0.022
1	48	0	40.972750	0.788	19	-0.019
1	58	0	40.972674	0.709	17	-0.020
1	43	+3	40.972486	0.680	17	-0.018
2	46	-3 & 3.3 pF	40.977182	0.688	17	-0.020
2	46	-3	40.980080	0.549	13	-0.014
2	49	0	40.980099	0.613	15	-0.015
2	59	0	40.979827	0.561	14	-0.015
3	83	-3 & 3.3 pF	40.976900	0.553	14	-0.011
2	63	+3	40.979662	0.560	14	-0.016
3	83	-3	40.980107	0.610	15	-0.011
3	50	0	40.980141	0.568	14	-0.014
3	60	0	40.979963	0.566	14	-0.011
3	82	+3	40.979724	0.419	10	-0.011

Table 6 Temperature sensitivity measurement results

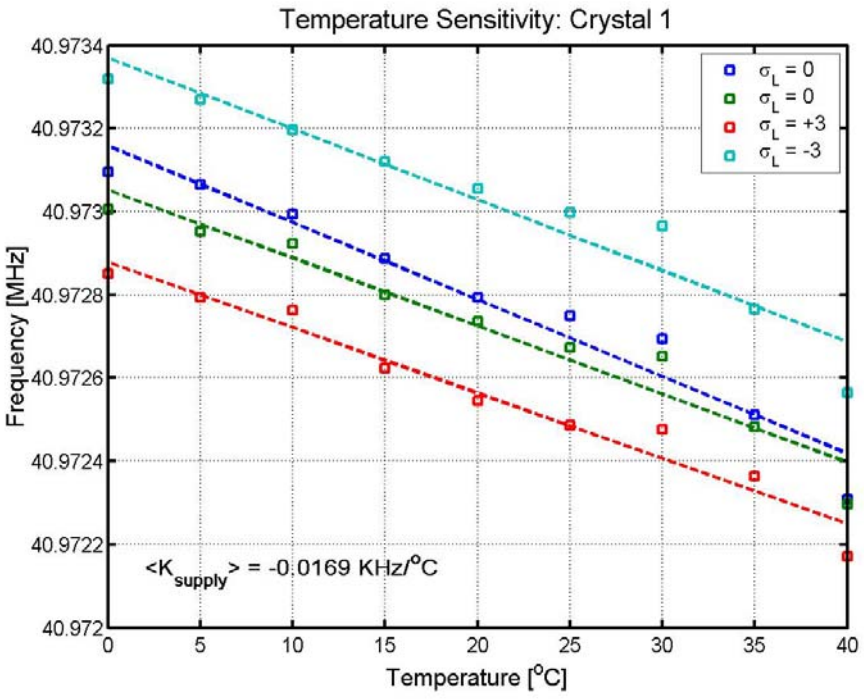


Figure 7 Temperature sensitivity measurement (crystal 1 with chips: 27, 48, 58 and 43)

Equivalent circuit capacitance

The circuit equivalent capacitance can be obtained from the crystal resonance frequency and the loaded frequency of oscillation. Table 7 reports this value for each tested chip. The mean value is 3.74 pF. This number should however be taken with care since it corresponds to crystal directly bonded to a naked chip. Thus, it does not take into consideration the package and layout parasitic capacitances.

Crystal Number	Chip Number	$\sigma_{process}$	Crystal Frequency [MHz]	Loaded Oscillation Frequency [MHz]	Frequency Shift [ppm]	$C_{circuit}$ @ 25°C [pF]
1	27	-3 & 3.3 pF	163.835554	163.881852	283	4.45 (+1.29)
1	27	-3	"	163.891992	344	3.16
1	48	0	"	163.891000	338	3.26
1	58	0	"	163.890696	336	3.30
1	43	+3	"	163.889944	332	3.38
2	46	-3 3.3 pF	163.847643	163.908728	372	5.22 (+1.27)
2	46	-3	"	163.920320	443	3.95
2	49	0	"	163.920396	444	3.95
2	59	0	"	163.919308	437	4.05
2	63	+3	"	163.918648	433	4.11
3	83	-3 & 3.3 pF	163.845441	163.907600	379	5.28 (+1.38)
3	83	-3	"	163.920428	457	3.90
3	50	0	"	163.920564	458	3.89
3	60	0	"	163.919852	454	3.96
3	82	+3	"	163.918896	448	4.04

Table 7 Estimation of the circuit equivalent capacitance

The following figures plot the circuit equivalent capacitance as function of the digital control number (Figure 8) and the control voltage (Figure 9).

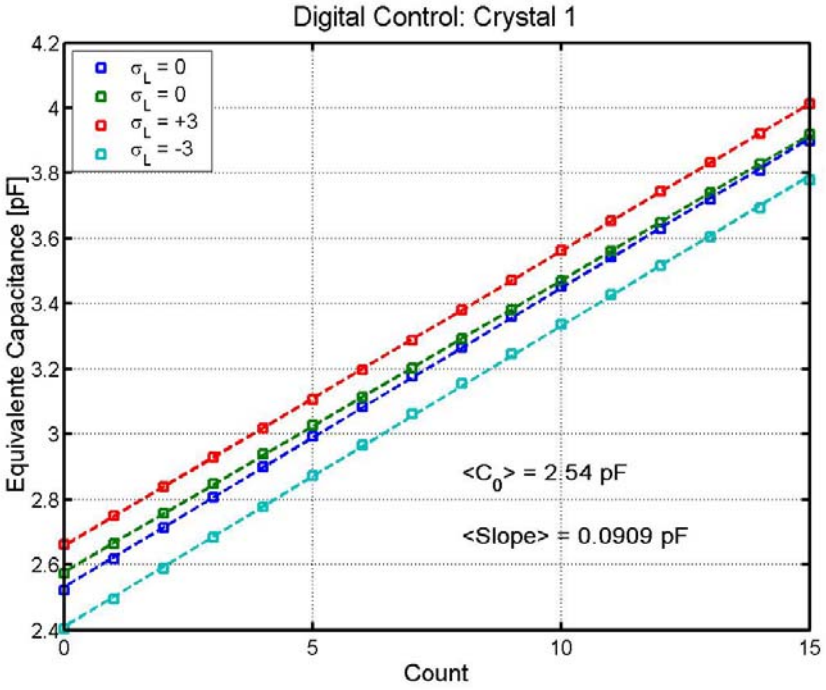


Figure 8 Circuit equivalent capacitance as function of the digital control number

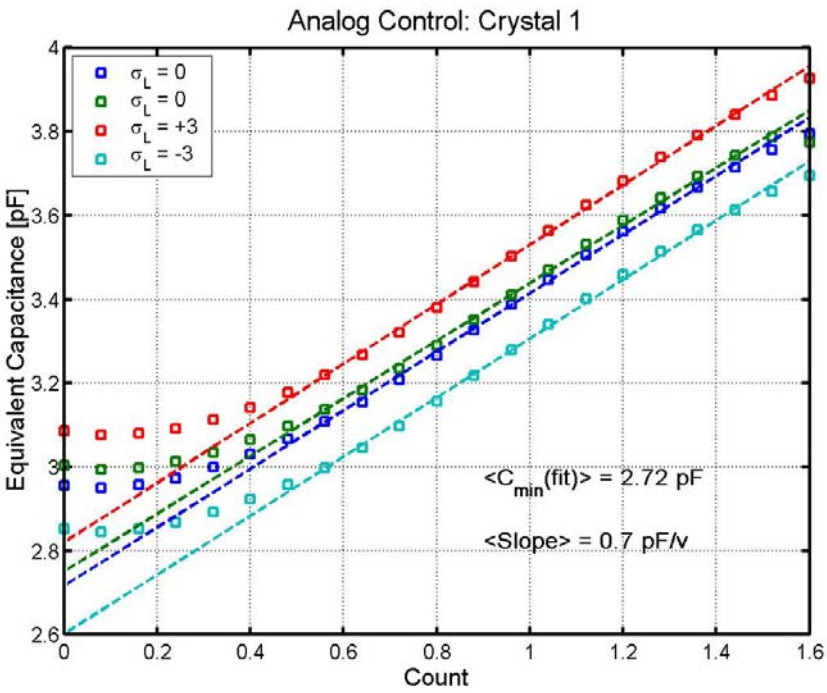
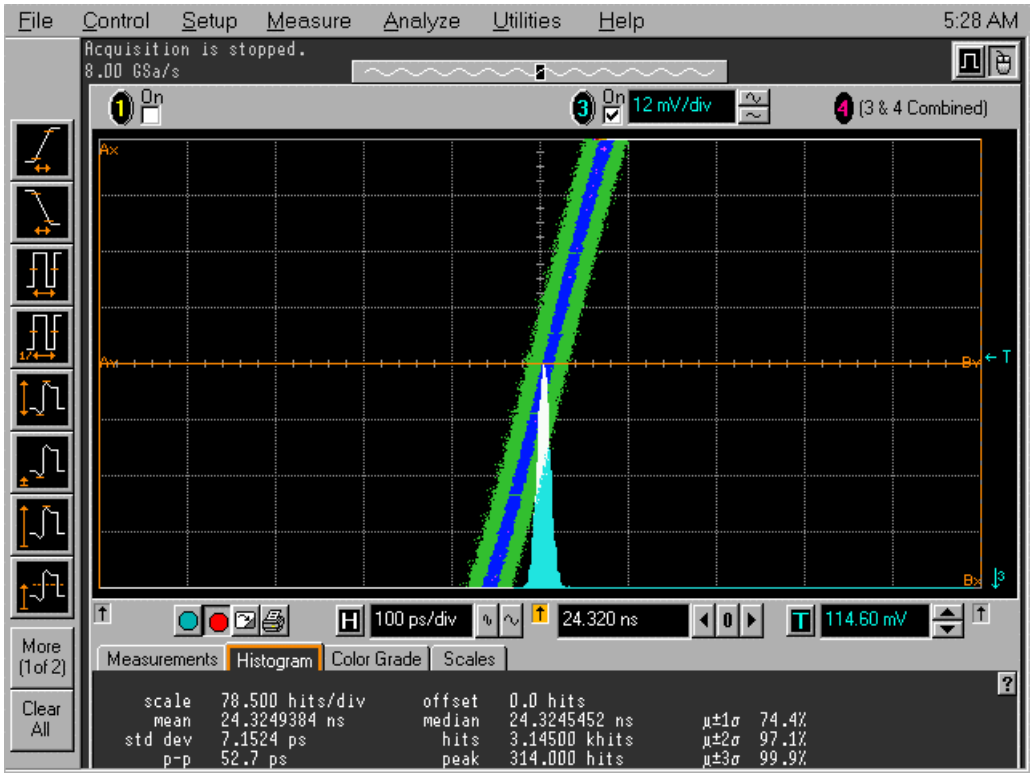


Figure 9 Circuit equivalent capacitance as function of the control voltage.

Cycle-to-cycle jitter



Crystal Specification

According to the latest data received from Bruce Taylor, the LHC RF frequencies are as follows:

- **Protons:**
  - 450 GeV: 400.78879 MHz
  - 7000 GeV: 400.78966 MHz
- **Lead ions:**
  - 450 GeV equivalent: 400.78406 MHz
  - 7000 GeV equivalent: 400.78964 MHz

A tolerance of ± 2 kHz applies in all cases.

The above numbers mean that the LHC RF frequency will be contained in between the following two values:

F(min) = 400.78406 MHz – 2 KHz = 400.78206 MHz
F(max) = 400.78966 MHz + 2 KHz = 400.79166 MHz

These correspond to the following center frequency and peak-to-peak deviation:

F(center) = 400.78686 MHz
ΔF = 24 ppm (±12 ppm)

The quartz crystal should thus be cut to have the following resonant frequency when loaded by the QPLL:

F(quartz) = 4 × F(center)/10 = 160.314744 MHz

The QPLL operation is such that at reset or "power on" the frequency calibration logic sets the digital control as close as possible to the LHC clock frequency. As can be seen from the measurements above (on the digital control), this should bring the oscillator frequency within ±3 ppm of the LHC frequency. The analog control is then used for final frequency and phase lock. The analogue control should allow to track any power supply and temperature variations occurring during normal operation. The analogue control tuning range should thus be excluded from the frequency budget calculation – this corresponds to a worst-case calculation. Additionally, due to IC fabrication process tolerances, the VCXO center frequency might be shifted from the ideal value by ±7 ppm. Given that this introduces an asymmetry in the tuning range, it is actually equivalent to a reduction of the VCXO tuning range.

Since the digital control allows a tuning range of ±50 ppm, the following frequency deviation can be tolerated for the crystal cutting accuracy, crystal temperature drift and aging (expected device life time 10 years):

ΔF(crystal) = ±50 ppm – (±3 ppm + ±12 ppm + ±7 ppm) = ±28 ppm

Temperature range: 0°C to +60°C

These numbers are preliminary and they certainly need to be reviewed once the QPLL is evaluated in its packaged and circuit layout.